Press Release

PR2017056

Socionext to Highlight Advanced SoC Design and Solutions at Annual DesignCon

Featuring High Performance SoC Designs including Ultra-High-Speed CMOS Transceiver, High-End Packaging Solutions and a Joint Technical Presentation on Advanced I/O Interface Design on Thursday, Feb. 2.

SUNNYVALE, Calif. Jan 18, 2017 --- Socionext Inc., a leader in state-of-the art system-on-chip technology, will feature its high performance SoC designs and advanced packaging solutions at the annual DesignCon Jan. 31 – Feb. 2 at the Santa Clara Convention Center, Booth 1239.

On February 2, Micron, Mentor Graphics and Socionext will jointly deliver a technical presentation focusing on SI Analysis of DDR Bus During Read/write Operation Transitions. Socionext will showcase its ultra energy-efficient 56Gb/s PAM4 and 56Gb/s NRZ analog and ADC-based SR to LR CMOS transceivers.

With the rapid growth of data traffic in data centers, 56+Gb/s signaling is being adopted for chip-to-module or chip-to-chip communications. Socionext provides a high-speed, yet energy-efficient transceiver with a 56Gb/s NRZ per lane power of 247mW/lane along with built-in test, debug and monitor features.

The company will also feature its 100+Gbps transceiver, which utilizes the company's ultra-high speed ADC & DAC technology, highlighting the power of converter-based architectures for high-bitrate applications.

The transceiver will be showcased at Socionext partners' booths.

In addition, the company, with extensive experience and expertise in quickly delivering high-quality package designs for high-speed, high-performance SoCs, will demonstrate its advanced "Chip-Package-PCB co-design" methodology, developed to help companies cost-effectively meet today's performance, functionality and time-to-market package design requirements.

During Track 7 on Feb. 2 at 4PM, a technical session on "Advanced IO Interface Design for Memory and 2.5D/3D/SiP Integrations" focusing on SI Analysis of DDR Bus During Read/write Operation Transitions will be jointly presented by Micron and Mentor Graphics in partnership with Socionext. The topic focuses on the critical challenges of (LP) DDRx buses with the shortening of time periods between the operations and simulating transitions from one to another, including read-to-write, write-to-read, and accesses to different ranks. The technical session will provide detailed findings and best practices on when and how to perform simulations to model operational transitions.

For the DesignCon website and programs, visit http://www.designcon.com/

About Socionext Inc.

Socionext is a new, innovative enterprise that designs, develops and delivers System-on-Chip products to customers worldwide. The company is focused on imaging, networking, computing and other dynamic technologies that drive today's leading-edge applications. Socionext combines world-class expertise, experience, and an extensive IP portfolio to provide exceptional solutions and ensure a better quality of experience for customers. Founded in 2015, Socionext Inc. is headquartered in Yokohama, and has offices in Japan, Asia, United States and Europe to lead its product development and sales activities. For more information, visit socionext.com.

For product information, visit the company's website at http://socionextus.com, e-mail sna_inquiry@us.socionext.com or call 1-844-680-3453. For company news and updates, connect with us on Twitter (https://www.twitter.com/socionextus) and Facebook (https://www.facebook.com/socionextus)

###

Press Contacts

Sherry Chen
Socionext America Inc.
1-408-737-5654
sna_pr@us.socionext.com

Dick Davies
IPRA
1-415-652-7515
ipra@mindspring.com