Custom SoC (ASIC)
Optimise the value of your products with Socionext’s custom SoC development

Talk to us about your custom SoC development needs. Socionext continues to expand its unique solutions for custom SoC development, reducing project risk and adding value to your products. Through our ability to support an increasing range of IP and process technology options, Socionext can address the needs of a wider range of customers and applications than ever before.
For customers considering their first SoC development, Socionext provides a range of support options. These include consulting services at all phases of the development, from initial concept definition to specification of the corresponding final SoC product. Our expertise in all aspects of the SoC design process, and our access to world-leading technologies enables us to partner with you in ensuring the optimal solutions to add value to your products.

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Custom SoC Solution

Reduce Risk and increase added value

Socionext’s custom SoC solution reduces the risk and minimize the timescales of new developments. We support our customers through the complete SoC design process to ensure project success. Previously, the benefits of custom SoC development were often outweighed by increased technical challenges due to the need for higher performance and complexity whilst minimizing power consumption. This led to high development costs and long project timescales.

Socionext’s SoC development solution is specifically aimed at addressing these issues, ensuring successful project completion whilst minimizing risk, cost and project duration. In addition to our position as one of the world’s leading custom SoC providers, we also offer a wide range of application-specific standard products (ASSPs) to the video- and image-processing, networking and information processing markets. Our ability to utilize design assets from these ASSPs in our customers’ SoC projects is a major factor in enabling the development of highly reliable custom SoCs in the shortest possible time – even for new SoC designs. How does this work? By combining silicon-proven, high value-add functional blocks from our ASSP products with our extensive IP portfolio, we can optimise the functionality of your custom SoC whilst significantly reducing development times and time-to-market for your products.

Socionext’s ASSP Products/Core Technologies
Developing a custom SoC based on an ASSP with a proven track record in the market not only makes it easy to design the components surrounding the CPU and the subsystems. It also has the advantage of easier development and evaluation because related software is also already provided.
Benefits of ASSP-based Development

Where a product is designed based on our ASSP product, the development period will be six months shorter than that by conventional design. We achieve this rapid time-to-market by shortening the hardware design period for SoC development and by developing software in advance.

- Delivery time of sample SoC: Six months ahead of schedule
- Advance development of software: Eight months ahead of schedule
- Product shipping: Six months ahead of schedule

Example of ASSP-based Development

This section introduces one example of ASSP-based development.

1. Extracting necessary application IP from ASSP
   - We extract application IPs which are required for customer’s development from our proven ASSP.

2. Combining base platform and extracted application IP
   - After cutting down unnecessary IPs and Interfaces from base platform, then we combine this optimise platform and extracted application IP.
Adding your special functions to differentiate from others
By adding your special functions to differentiate from others, your special SoC design is now created.

Evaluating and verifying functions, performance, and power
The functions, performance, and power can be evaluated and verified using a dedicated hardware emulator at approximately 1000 times as fast as an HDL simulator.
For your software development, we provide a prototype environment such as an FPGA board and CPU board. This allows customers to develop software before manufacturing SoC.

PCB (printed circuit board) co-design
Implementing high-speed components (DDR, PCIe, USB, etc.) and SoC on a PCB tends to cause a electrical issue such as electromagnetic noise, crosstalk, and clock jitter. We analyze such issue creating PCB prototype and offer proposed measures.
This reduces risk associated with developing a PCB and thereby reduces cost for PCB design and manufacturing.

Full Custom Development
To achieve the best performance of your SoC, we have full custom development option that allows you to customize as you like. For your full custom SoC development, we fully support for 1. proposing system architecture, 2. providing subsystem and a various of IPs, 3. optimized CPU peripheral design, and 4. system verification by hardware emulator and FPGA prototype. We also provide a device driver development service under contract as part of our software development support.
At Socionext, we apply an optimized flow according to the features of the SoC to be developed, according to the following design flow.
### Custom SoC Solution

#### Interface with Customer

<table>
<thead>
<tr>
<th>Specification I/F</th>
<th>RTL I/F</th>
<th>Netlist I/F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Customer</td>
<td>Customer</td>
<td>Customer</td>
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<tr>
<td>Socionext</td>
<td>Socionext</td>
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</table>

#### Contents

- **Consulting service**
- **Development support service**
- **Provision of subsystems**
- **Provision of IP**
- **Design technology**

#### Planning

1. **Planning**
2. **Specification**
3. **Logic Design**
4. **Logic Synthesis**
5. **Physical Design**
6. **Verification**
7. **Testing/Shipment**

#### Consulting service

- Brainstorming design ideas
- Consulting design direction
- Provision of ASSP creation service
- SIC logic design service
- High-speed logic verification service
- Software development service
- Low power consumption technology
- Provision of subsystems

#### Development support service

- RTL co-design support service
- PCB co-design support service
- Chip package co-design service
- Power supply/crosstalk analysis
- Packaging/manufacturing technology
- Design planning

#### Provision of subsystems

- System-level design
- Requirement specification formulation
- Development planning
- System specification formulation
- Function verification
- Logic synthesis
- Verification
- Design planning
- Test circuit insertion
- Creating prototyping board

#### Provision of IP

- FPGA fitting
- Board selection/
- New development FPGA prototyping

#### Design technology

- Gate simulation
- Variation timing analysis
- Crosstalk noise analysis
- Physical verification
- Power rail analysis
- Power consumption analysis
- Sample shipment
- Mass-production shipment
- Lithography verification
- Algorithm design
- SystemC rewriting
- High-level synthesis RTL design
- Front-end design
- Back-end design
- DFT
- Sign-off

#### Software development service

- Specification formulation
- Test design
- OS migration
- Boot development
- Driver development
- App development
- PCB Specification formulation
- PCB prototyping
- PCB design
- Creating evaluation board with ES
- Evaluating evaluation board with ES
- Test pattern generation

#### PCB co-design support service

- Mode-corner optimization
- Physical aware synthesis
- Physical aware design
- Power aware design
- Power supply/crosstalk analysis
- Packaging/manufacturing technology
- Design planning
- Test circuit insertion
Socionext provides the three types of basic design interface shown below. The optimal combination of customers’ design assets and our design technologies improves the efficiency of SoC development projects. We also provide a design flow that incorporates upstream verification and FPGA prototyping, supporting ever higher-quality projects and shorter development periods.

### Three Types of Development Interface

- **Specification interface**
  The specification interface method is used to interface with the customer based on the SoC design specifications. The customer will prepare a design specification document for the SoC to be developed. We will create an SoC development specification document based on those specifications, verify the logic design, and take care of everything right through to delivery of the SoC.

- **Interface RTL**
  The interface RTL method is used to interface with the customer based on design data (RTL) created by the customer through functional design. The customer will perform functional design through to verifying RTL. We will examine the test specifications, build a test circuit, and manage all processes through to SoC delivery.

- **Netlist interface**
  The netlist interface method is used to interface with the customer based on a netlist composed of our cells. The customer will perform tasks up to logic synthesis for netlist creation.
Development Support Service (DesignExpress™)

This design service provides you with consistent development support for everything from system specification to evaluation, as well as for PCB design, in every facet of custom SoC development. This service enables you to focus on your product development while shortening the development period, reducing risks associated with reworking, improving product quality, and reducing power consumption.

List of Development Support Services

- Virtual environment creation service (Cedar™-ESL)
- High-level synthesis support service (Cedar™-HLS)
- SoC logic design service
- High-speed logic verification service (Cedar™-EMU)
- Prototype board development service (Cedar™-PROT)
- PCB co-design support service (PLACATE™)
- Software development service
Virtual environment creation service (Cedar™-ESL)

When considering SoC specifications and architecture, you only need to choose the services you actually need. Select from the following four menu items from the virtual environment creation service.

- Virtual environment creation service for feasibility studies
- Environment for measuring detailed bus architecture performance + Performance evaluation
- Environment for advance development of software
- Environment for software-driven performance evaluation

<table>
<thead>
<tr>
<th>Service Category</th>
<th>Service Description</th>
<th>Item Submitted by Customer</th>
<th>Deliverable from Socionext (Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provide of development environment for advance development of software</td>
<td>A virtual platform for software development is provided</td>
<td>Block diagram Block functional specification</td>
<td>High-speed virtual platform (for software development)</td>
</tr>
<tr>
<td>Provide of environment for software driven performance evaluation</td>
<td>A virtual platform for software driven performance evaluation is provided</td>
<td>Block diagram Block functional specification Software scenario</td>
<td>High-speed virtual platform (for architecture design)</td>
</tr>
<tr>
<td>Provide of environment for detailed architecture performance evaluation</td>
<td>A virtual platform for architecture performance evaluation is provided. Performance is measured</td>
<td>Architecture construction diagram Evaluation scenario</td>
<td>High-accuracy virtual platform Performance measurement report</td>
</tr>
</tbody>
</table>
High-level synthesis support service (Cedar™-HLS)

The high-level synthesis support service rewrites source code and provides a library that can be synthesized with that code. This tunes your source code into a high-level language (SystemC/C/C++) for adaption to the applicable process technology. After checking the consistency between the high-level synthesis results and the process technology to be used, we provide you with rewritten source code and the like.

### Cedar™-HLS Service Outline

<table>
<thead>
<tr>
<th>Customer’s tasks</th>
<th>Socionext’s tasks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Algorithm C/C++</td>
<td>Code, high level synthesis constraints, verification report</td>
</tr>
<tr>
<td></td>
<td>High level synthesis optimization/verification</td>
</tr>
<tr>
<td>High level synthesizable C/C++</td>
<td>Library</td>
</tr>
<tr>
<td>Verification of high level synthesis</td>
<td>RTL Rule Set</td>
</tr>
<tr>
<td>RTL Style Check</td>
<td>RTL Style Check</td>
</tr>
<tr>
<td>Logic synthesis</td>
<td>Logic synthesis</td>
</tr>
<tr>
<td>Netlist</td>
<td>Equivalence verification</td>
</tr>
<tr>
<td>Placement and routing</td>
<td></td>
</tr>
<tr>
<td>Provided</td>
<td>Netlist</td>
</tr>
<tr>
<td>RTL hand-off</td>
<td></td>
</tr>
<tr>
<td>Netlist hand-off</td>
<td>Netlist</td>
</tr>
<tr>
<td>RTL Rule Set</td>
<td></td>
</tr>
<tr>
<td>Netlist</td>
<td></td>
</tr>
<tr>
<td>Placement and routing</td>
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</table>

### Service Category

<table>
<thead>
<tr>
<th>Service Category</th>
<th>Service Description</th>
<th>Item Submitted by Customer</th>
<th>Deliverable from Socionext (Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Handing off of RTL designed with high level synthesis RTL hand-off</td>
<td>Rewriting of a language in accordance with the tool</td>
<td>Functional specifications, Constraint conditions, High level language</td>
<td>Rewritten high level language, Library for high level synthesis, RTL designed with high level synthesis</td>
</tr>
</tbody>
</table>

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**Development Support Service**

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**SoC logic design service**

With the SoC logic design service, Socionext will do the logic design on your behalf. In addition to complete SoC design, we can also do partial design. By combining various functional macros that we handle, we provide design data that best suits your system. Note that design data includes a functional specification document, RTL, and a verification report.

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**SoC Logic Design Outline**

1. **Customer’s logic system requirements**
2. **SoC specifications**
   - CPU, IP
   - Bus configuration
3. **Verification plan**
   - Verification method
   - Operation scenario
4. **Customer’s logic review & approval**
5. **RTL design**
6. **Functional verification**
7. **Performance verification**
8. **Verification specifications**
9. **Verification result reports**
10. **Customer’s logic review & approval**

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**Application Example of SoC Logic Design Service**

Software block diagram
- Extract functions required for applications
- Mass storage class
- TCP/IP protocol stack
- RTOS
- USB HOST driver
- Ethernet driver

Memory map
- TCM
- FLASH
- I/O
- SRAM
- DRAM

CPU selection
- Cache capacity
- SRAM capacity

Bus topology
- FIFO, QoS

HW/SW coordination
- Dedicated hardware assist line

Inter Connect (AXI/AHB/APB)

CPU Block
- CPU
- DMAC
- SRAM

Storage Block
- USB
- SDIO

Network Block
- DDR Controller
- Network
- Security
- GMAC
- PCIe

User Block
- UDL-A
- UDL-B

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<table>
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</tr>
</thead>
<tbody>
<tr>
<td>SoC Logic Design</td>
<td>Specification design</td>
<td>Requirement specifications</td>
<td>SoC specifications</td>
</tr>
<tr>
<td></td>
<td>RTL design</td>
<td>Macros to be installed</td>
<td>RTL</td>
</tr>
<tr>
<td></td>
<td>RTL verification</td>
<td>Functional and performance requirements</td>
<td>Verification specifications, result reports</td>
</tr>
</tbody>
</table>
High-speed logic verification service (Cedar™-EMU)

The high-speed logic verification service uses emulators and the like to perform high-speed logic verification and compute SoC power consumption. We can prototype a circuit by mapping a circuit of the system to be developed to an emulator. It can also compute your proposed system's power consumption. Since the emulator runs 500 to 1,000 times faster than a software simulator, you can significantly reduce verification time.

Cedar™-EMU Service Outline

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<tr>
<td>Chip level verification</td>
<td>Formulation of verification specifications</td>
<td>Outline block diagram</td>
<td>Verification specifications</td>
</tr>
<tr>
<td></td>
<td>Creation of verification data</td>
<td>Design data (RTL or netlist)</td>
<td>Verification data</td>
</tr>
<tr>
<td></td>
<td>Construction of verification environment</td>
<td>Input/expected value data</td>
<td>Emulation verification results</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>System level verification</td>
<td>System level verification using software developed in an ESL environment</td>
<td>Design data (RTL or netlist) Input/expected value data Test programs</td>
<td>Emulation verification environment Verification result reports</td>
</tr>
<tr>
<td>Power consumption reduction</td>
<td>Measurement of power consumption</td>
<td>Power measurement program</td>
<td>Reports on results of power consumption measurement</td>
</tr>
</tbody>
</table>
Prototype Board Development Service (Cedar™-PROT)

The prototype board development service provides a prototype board for system-level verification and advance development of software. By implementing an IP equivalent to the IP to be installed on the system on an FPGA, this service provides a board that is equivalent to the target system. Since we can perform system-level verification and advanced software development before the SoC is completed, you can improve its quality and shorten the development period.

- System development that enables verification on actual equipment
- High equivalence with custom SoC
- Prototype development using custom SoC IP
- Arm core can also be implemented
- Software development technology
  - IP verification with implemented driver
  - Software platform can be provided
- Board design technology
  - Printed board design supporting high-speed interface
- Custom SoC/FPGA design technology
  - Logic design based on presented specifications

Record of applications of Cedar™-PROT
- Controller custom SoC for network
- Image processing custom SoC for documents
- Custom SoC for measuring instruments
- Many others

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<th>Item Submitted by Customer</th>
<th>Deliverable from Socionext (Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>System level verification</td>
<td>Provide of a prototype board</td>
<td>Requirement specifications (specified circuit information, etc.)</td>
<td>Board unit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board specifications</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FPGA ROM data</td>
</tr>
</tbody>
</table>
PCB Co-design Support Service (PLACATE™)

The PCB co-design support service analyzes noise and supports countermeasures based on an integrated SoC and PCB model that help you to significantly shorten the system development period and reduce costs through reduced BOM. By applying this service from the upstream phase of custom SoC design and PCB design, we help to cut your design time by reducing the amount of SoC and PCB design rework that needs to be done, thereby improving their systems and significantly shrinking the evaluation workload.

### Design Flow Image

#### During custom SoC development

- **Prototyping**
  - CHIP design
  - PKG design
  - PCB design
  - Analysis and measures with PLACATE™

- **Actual design**
  - CHIP model
  - PKG model
  - PCB model
  - Verification with PLACATE™

#### After custom SoC development

- **Simulation Kit**
  - CHIP model
  - PKG model
  - PCB model
  - Difference analysis with "during custom SoC development"

- **Further support**
  - PCB model
  - Product A
  - Product B

### Service Description

- **Board prototyping**
  - Wiring/Reducing bypass capacitors
  - Integrated noise analysis for SoC, PKG, and Board
  - DRAM-IF (DDR4, etc.) SI/PI analysis
  - SerDes (PCIe Gen3, etc.) SI analysis
- **Creation of SoC power supply models**
  - LPM+IBIS5.0
- **Looking into measures for EMC**
  - Consulting by INARTE engineers

### Deliverable (Example)

- Board design guidelines
- Board reference design
- SI/PI analysis result reports
- SoC power supply model (LPM + IBIS5.0)
- EMI analysis results
- EMI countermeasure proposals

### Structure of Simulation Kit

#### Simulation Kit

- Measurement
- Simulation

#### Simulation Deck

- Simulation Kit
  - Reference Design
  - Simulation Parameters

### Case of Bypass Capacitor Reduction

- **Initial proposal**
  - 100%
- **Confirmed**
  - That capacitors can be reduced by up to 20% of the initial proposal based on the integrated chip-package-PCB verification
- **50%**
- **25%**
- **0%**

### Case of EMI Analysis

- **Near Field**
- **Far Field**
Software Development Service

When reviewing the hardware specifications, it is important to examine the factors that form the basis of your SoC, such as the system startup sequence and power-saving features. Also, after deciding on the specifications, these need to be embodied in software and checked in terms of the logic verification and board verification phases. Socionext works with you during such phases from the perspective of software development, and supports you in specification design through to board evaluation. All this produces a system that is consistent across hardware and software, ensuring reliability.

[DPI (Device Programming Interface)]

DPI is an IP operation sequence in which a group of functions, including initialization, starting operation, and stopping an IP macro, is written into software, and for which the operation check has been completed. You can use DPI in various development phases in the following ways:

- To check IP operation at an early stage (to be reflected in hardware verification scenarios)
- To develop device drivers in a short time (assisting the user in understanding specification documents, use of API)
- To quickly evaluate engineering samples (IP communication check, analysis)

[Subsystems]

Various types of subsystem are available for use as the foundation for support services. For details, see the section on subsystems.


**Subsystem Service**

**Provide of Subsystems**

Socionext provides subsystems featuring specific functions enabled by combining various types of IP. By incorporating a subsystem, the main system can achieve high performance with a specific function and low power consumption.

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**Image Signal Processor Subsystem**

**Background and Initiatives**

Under the current circumstances where camera solutions continue to advance, it is extremely difficult to keep providing new functionality and offering differentiating features every year. We have created IP for the image macro part of our image signal processor (Milbeaut®) with a track record of 18 years and provide it as a high-resolution, high-performance subsystem.

**Outline**

By creating IP for an image macro for each functional block, it is possible to build a flexible platform. Each IP has the AXI interface so SoC integration is easy.

**Features**

- High-performance 4Kp60 600Mpix/sec (ex TSMC 28nm HPC+)
- API for effectively using image macros is provided.
- An image adjustment simulator is provided to emphasize the individuality of images.

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**Lineup**

<table>
<thead>
<tr>
<th>IP Block</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2B</td>
<td>Bayer domain processing</td>
</tr>
<tr>
<td>B2R</td>
<td>Demosaic processing</td>
</tr>
<tr>
<td>LTM</td>
<td>Local tone mapping</td>
</tr>
<tr>
<td>R2Y</td>
<td>RGB to YUV conversion</td>
</tr>
<tr>
<td>CNR</td>
<td>Color noise reduction</td>
</tr>
<tr>
<td>3DNR</td>
<td>Multi-frame noise reduction</td>
</tr>
<tr>
<td>HDR</td>
<td>High dynamic range synthesis</td>
</tr>
<tr>
<td>LDC</td>
<td>Lens distortion correction</td>
</tr>
</tbody>
</table>

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**Low light intensity noise reduction**

![400lux](image1.png) ![0.01lux](image2.png)

**Defective pixel correction**

![Corrected image](image3.png)

**Lens distortion correction**

![Corrected image](image4.png)
Arm® Processor Core Subsystem

Arm Cores and Design Kits

The comprehensive license agreement with Arm allows customers to select the most suitable Arm core to meet their requirements. We provide the most suitable Arm core and SNAP-DK (design kit), a design environment, for custom SoC for a wide range of applications such as microcontrollers, embedded device, and application equipment.

These Arm Cores in the line-up are available on all process technologies that Socionext offers.

Socionext Arm Platform (SNAP)

Use of the SNAP (Socionext Arm based SoC Platform) reduces development time and risks in Arm core-based SoC development. SNAP consist of the following.

● Design Kits: SNAP-DK, ADK, SDK
  ● SNAP-DK: Consists of an Arm core and minimum required peripheral IPs.
  ● SNAP-ADK: SNAP-DK-based design kit that al-ready implements an interface macro, GPU, etc.
  ● SNAP-SDK: This design kit provides a fully customized dedicated subsystem for customers using a design tool in accordance with the requirement specifications.

By selecting the most suitable design kit based on the specifications customers require, development time can be reduced significantly. These design kits, containing a simulation environment, test bench, sample boot code, etc., contribute to the shortening of time to launch the design environment and creation of an appropriate Arm core boot program.

● Prototyping: SNAP-PK
  ● The SNAP-PK provides Socionext’s unique FPGA board with SNAP-DK. By implementing a user logic on the FPGA side, it achieves prototyping of an SoC.
  ● This product can be used for system operation verification of hardware, performance evaluation, and early development of software.

### Line-up of Arm Core, GPU and SNAP-DK

<table>
<thead>
<tr>
<th>Arm core</th>
<th>Arm v4, v5, v6</th>
<th>Arm v7</th>
<th>Arm v8</th>
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</thead>
<tbody>
<tr>
<td>● Arm11</td>
<td>Cortex-A</td>
<td>Cortex-A75/A72</td>
<td></td>
</tr>
<tr>
<td>● Arm9</td>
<td>Cortex-R</td>
<td>Cortex-A72</td>
<td>Cortex-A55</td>
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<tr>
<td>● Arm7</td>
<td>Cortex-M</td>
<td>Cortex-A53</td>
<td>Cortex-A35</td>
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<table>
<thead>
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<th>GPU</th>
<th>Utgard</th>
<th>Midgard</th>
<th>Bifrost</th>
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<tr>
<td>● Mali-400</td>
<td>T820</td>
<td>G71</td>
<td></td>
</tr>
<tr>
<td>● T620</td>
<td>G51</td>
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<table>
<thead>
<tr>
<th>SNAP-DK</th>
<th>DK-11</th>
<th>DK-Av7</th>
<th>DK-Av8(A53)</th>
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<tbody>
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<td>DK-Rv8</td>
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<td>DK-7</td>
<td>DK-Mv7</td>
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### SNAP Design Kits

<table>
<thead>
<tr>
<th>Type</th>
<th>Content</th>
<th>Advantage</th>
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</thead>
<tbody>
<tr>
<td>SNAP-DK (Basic Design Kit)</td>
<td>CPU + small-scale peripheral IPs</td>
<td>Bootable CPU subsystems can be used</td>
</tr>
<tr>
<td>SNAP-ADK (Advanced Design Kit)</td>
<td>SNAP-DK + high performance IPs (system with guaranteed performance)</td>
<td>High performance CPU subsystems including an OS can be used</td>
</tr>
<tr>
<td>SNAP-SDK (System Design Kit)</td>
<td>Consultation-based full custom design kit (system with guaranteed performance)</td>
<td>Dedicated subsystems based on requirement specifications and existing systems can be used</td>
</tr>
</tbody>
</table>

### SNAP-PK

SNAP-PK provides Socionext’s unique FPGA board with SNAP-DK. By implementing a user logic on the FPGA side, it achieves prototyping of an SoC. This product can be used for system operation verification of hardware, performance evaluation, and early development of software.
Background and Initiatives
Due to an imbalance between the advance of DDR memory to the ultra-high speed generation along with an increase in the burst length and access by video codec processes handling small size rectangular image data to the DDR, a reduction in the efficiency of using the DDR memory band width has become an issue. This subsystem enables high efficiency video codec processing that can save the band width using Socionext’s unique technology.

Outline
We have developed our unique bus protocol methodology that can improve memory access efficiency in the codec process without being significantly affected by advances in DDR. Tightly coupling our codec engine and our memory controller with the methodology enables the memory controller to efficiently access DRAM by taking into account a physical memory map based on the 2D information on image data accessed by the codec engine, reducing the required memory band width significantly.

Features
- Achieves various types of HEVC codec processing with a smaller bus width (bit) as listed below.

<table>
<thead>
<tr>
<th>Processing details</th>
<th>Socionext’s conventional system</th>
<th>Video codec subsystem</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>4k 60p 4:2:2 10bit</td>
<td>112bit</td>
</tr>
<tr>
<td></td>
<td>4k 60p 4:2:2 10bit</td>
<td>96bit</td>
</tr>
<tr>
<td></td>
<td>4k 60p 4:2:0 8bit</td>
<td>64bit</td>
</tr>
<tr>
<td>Encode</td>
<td>4k 60p 4:2:2 10bit</td>
<td>96bit</td>
</tr>
<tr>
<td></td>
<td>4k 60p 4:2:0 10bit</td>
<td>80bit</td>
</tr>
<tr>
<td></td>
<td>4k 60p 4:2:0 8bit</td>
<td>64bit</td>
</tr>
</tbody>
</table>

Example: When using LPDDR4 2400 Mbps

General Relationship between Codec IP Core and DDR Memory

Relationship between Socionext Codec IP Core and DDR Memory
IP Video Streaming Subsystems

Background and Initiatives
With the spread of the Internet, demand for video streaming is exploding. Typical examples are media servers for downstreaming and network monitoring cameras for upstreaming. In such target areas, Socionext carries out fragmentation and IP packetization of video data after codec processing, significantly reducing the processing load of the main system.

Outline
This subsystem encapsulates video and audio data into an IP packet and encapsulates the IP packet into an Ethernet frame. The high-performance IP macro executes the following series of processes just by placing data after codec processing.

- Packetizing video data (ES: elementary stream, loaded into DRAM) into TS packets
- Encapsulating ES, TS, or JPEG data into RTP packets
- Encapsulating RTP packets into IP packets
- Encapsulating IP packets into Ethernet frames and performing GMAC control (video transmission)

Features
- Support for RTP/UDP offloading
  [Supported formats]
  - ES over RTP: Video (H.264), Audio (G.771, AAC)
  - JPEG over RTP
  - TS over RTP
  - Metadata over RTP
- Support for Max. 32 streams
- Integration with security (encryption) functionality

<table>
<thead>
<tr>
<th>Transfer band (Mbps)</th>
<th>10</th>
<th>30</th>
<th>50</th>
<th>150</th>
<th>300</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offloading not available</td>
<td>23</td>
<td>62</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU load factor (%)</td>
<td>15</td>
<td>21</td>
<td>29</td>
<td>39</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Actual measurement of products
Load reduced by 25 times
Background and Initiatives

The HDMI 2.1 specifications were defined in 2017. It has 48-Gbps bandwidth, 2.7x that of conventional HDMI 2.0, and enables the transmission of extremely large data sets, including 8K video, with very low latency while maintaining high image and sound quality. With our extensive knowledge in developing data-transmission technologies for consumer video equipment such as recorders and 4K TVs, as well as for high-speed, serial data transmission used in large-scale servers, Socionext offers the world’s first HDMI 2.1 compatible data transmission and reception subsystem (Link/PHY).

Outline

This subsystem supports the HDMI 2.1 (High-Definition Multimedia Interface) specification. It supports video resolution of up to 4320 x 7680p and color depth of 8, 10, and 12 bits, and covers a bandwidth of 48 Gbps. While supporting L-PCM audio data and compressed audio data, the subsystem supports high bit-rate audio (up to 768 kHz) as well as sampling rates from 32 kHz to 192 kHz.

Features

- Support for VESA DSC 1.2a
- Support for Dynamic HDR and eARC
- Support for game mode VRR/QMS
- Support for HDCP2.2
- Support for hot plug detection

[Example: HDMI 2.1 Receiver PHY/Link]
**Power-saving Subsystem**

**Background and Initiatives**

In step with SoCs becoming more functional and highly integrated recently, providing a power-saving mode has become an absolute essential. For example, network standby mode keeps the minimum required interfaces, mainly network functions, awake and places the remaining functions in standby to save power. Sleep mode keeps only subsystems awake to make the system enter a deeper sleep, and there are various ways to implement power-saving mode. We provide a power-saving system to satisfy such needs.

**Outline**

A power-saving subsystem is composed of an Arm microcomputer, minimum required peripheral IP, RAM, and others, and operates separately from the main system. By doing so, this subsystem allows you to achieve the following functions.

- Transition and return from power-saving mode with a simple instruction from the main system to the subsystem
- Achieve deep-sleep mode by keeping only the subsystem awake
- Integrate the power-up and shut-down sequences

---

**During Operation**

- **SoC**
  - Main system (CPU)
  - Power Domain A
  - Power Domain B
  - DRAM
  - PMIC
  - Unified control of internal/external power, clock, and reset

**Power-saving Mode**

- **SoC**
  - Main system (power-saving mode)
  - Power-saving subsystem
  - PMU
  - CRG

Maintaining and returning from the power-saving condition by the microcomputer

---

We offer the following support services that make it easy to introduce the subsystem.

- Support for considering system power-saving sequences between the main system and subsystem
- Software design support for main system sleep and wake-up scenarios
- Design support for controlling the subsystem power supply
Network Standby Response

Network standby response is a function in which the subsystem carries out packet processing on behalf of the main system when it is in a standby state. This function also supports the following functions.

[Supported functions]
- Main system wake-up assistance when a packet requiring processing by the main system is received
- The acceleration function that accelerates packet processing in a normal state

Network Standby Response Outline

<table>
<thead>
<tr>
<th>Main system</th>
<th>Power-saving subsystem</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU (x n) (AP)</td>
<td>CPU (microcomputer)</td>
</tr>
<tr>
<td>DMAC</td>
<td>SRAM</td>
</tr>
<tr>
<td>User Logic1</td>
<td>GMAC</td>
</tr>
<tr>
<td>MEMORY Ctrl.</td>
<td>PHY</td>
</tr>
</tbody>
</table>

During system standby: Maintains network functionality by using the subsystem’s firmware
During normal times: Provides a network acceleration function from the standby response FE

Actual Network Standby Response Performance Values

<table>
<thead>
<tr>
<th>Function/Performance</th>
<th>Normal</th>
<th>When using proprietary technology</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stand-by power</td>
<td>2 W to several W</td>
<td>&lt;100mW</td>
<td>&lt;1/20</td>
</tr>
<tr>
<td>Communication performance</td>
<td>300Mbps</td>
<td>900 Mbps (20% reduction in CPU load)</td>
<td>Approx. 3 times</td>
</tr>
</tbody>
</table>

Actual measurements with MB86S73 board
Security Subsystem

● Background and Initiatives
With the recent progress of the IoT (Internet of Things), a security system has become an essential item. Although a high level of protection for secret information and high-speed algorithm processing by hardware are indispensable for a security system, it is not easy to develop such hardware and software from scratch. Using Socionext’s security subsystem can reduce the burden of such development, making it possible for you to introduce a security system efficiently.

● Outline
The security subsystem includes a dedicated key storage box to store highly secret key information. It also incorporates a hardware engine that uses the stored key to perform high-speed encryption and authentication processing, achieving a high-level security system.

[Features of the security subsystem]
① Secure key generation and input through a dedicated e-mail box
② Secure key storage through locating key storage in a module
③ A dedicated engine that uses a key in a secure key storage box

The following presents an example function using this subsystem and system configuration.

● Example Function Using Subsystem: Secure Boot
The boot code is executed at the beginning of system startup, and whether a correct program is used or not must be examined on the basis of the boot code. It is the key for a security system where such important code is encrypted and stored, and a mechanism is in place to detect whether such code has been altered. The security subsystem provides a mechanism to protect and securely execute such important code.
● Example of System Configuration Using Subsystem

The security subsystem can be applied as follows for the entire system.

① Secure boot from a micro computer in a secure sub-block and ROM
② Creation of a dedicated key storage route and encryption processing for a non-secure main block
③ Key management for another encryption engine by using the security subsystem and a microcomputer in a secure sub-block

● Hardware Accelerator

The following shows a list of security algorithm accelerators installed in the subsystem.

<table>
<thead>
<tr>
<th>System</th>
<th>Key Length (bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common key encryption</td>
<td></td>
</tr>
<tr>
<td>3DES-ECB</td>
<td>168</td>
</tr>
<tr>
<td>3DES-CBC</td>
<td>168</td>
</tr>
<tr>
<td>AES-ECB</td>
<td>128/192/256</td>
</tr>
<tr>
<td>AES-CBC</td>
<td>128/192/256</td>
</tr>
<tr>
<td>AES-CTR</td>
<td>128/192/256</td>
</tr>
<tr>
<td>AES-GCM</td>
<td>128/192/256</td>
</tr>
<tr>
<td>Hash</td>
<td></td>
</tr>
<tr>
<td>SHA-1</td>
<td>–</td>
</tr>
<tr>
<td>SHA-256</td>
<td>–</td>
</tr>
<tr>
<td>SHA-512</td>
<td>–</td>
</tr>
<tr>
<td>HMAC</td>
<td></td>
</tr>
<tr>
<td>SHA-1</td>
<td>160</td>
</tr>
<tr>
<td>SHA-256</td>
<td>256</td>
</tr>
<tr>
<td>SHA-512</td>
<td>512</td>
</tr>
<tr>
<td>Electronic signature</td>
<td></td>
</tr>
<tr>
<td>generation/verification</td>
<td></td>
</tr>
<tr>
<td>RSA</td>
<td>2048 - 3072</td>
</tr>
<tr>
<td>ECDSA</td>
<td>256/384/521</td>
</tr>
</tbody>
</table>
## IP Macro Service

### Line-up of IP Macros

Socionext’s IP macros with their proven track records support customers in advanced SoC development.

#### Functional/Interface Macros

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>Process Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>90nm</td>
</tr>
<tr>
<td>Arm Cores</td>
<td>Cortex-A</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Cortex-R</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Cortex-M</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Arm11, Arm9, Arm7</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Mali</td>
<td>✓</td>
</tr>
<tr>
<td>Image Core</td>
<td>JPEG</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>H.264</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>H.265</td>
<td>✓</td>
</tr>
<tr>
<td>Security Core</td>
<td>SHA</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>PKA</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>3DES</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>AES</td>
<td>✓</td>
</tr>
<tr>
<td>Interface Controller Core</td>
<td>OSPI/QSPI</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td>✓</td>
</tr>
<tr>
<td>SD</td>
<td>UHS-I</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>UHS-II</td>
<td>✓</td>
</tr>
</tbody>
</table>

#### High Speed Interface Macros

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>Process Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>90nm</td>
</tr>
<tr>
<td>USB</td>
<td>USB3.1 Gen2 Host/Device</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>USB3.1 Gen1 (USB3.0) Host/Device</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>USB2.0 Host/Hub/Device</td>
<td>✓</td>
</tr>
<tr>
<td>Ethernet</td>
<td>Gigabit Ethernet MAC</td>
<td>✓</td>
</tr>
<tr>
<td>Video</td>
<td>HDMI2.0</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>V-By-One HS</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>FPD-Link</td>
<td>✓</td>
</tr>
<tr>
<td>LVDS</td>
<td>LVDS</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>SubLVDS</td>
<td>✓</td>
</tr>
<tr>
<td>MiPI</td>
<td>DSI TX</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CSI-2 TX/RX</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>D-PHY</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>C/D-PHY</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>M-PHY</td>
<td>✓</td>
</tr>
<tr>
<td>PCI Express</td>
<td>PCIe Gen4 RT/EP</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>PCIe Gen3 RT/EP</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>PCIe Gen2 RT/EP</td>
<td>✓</td>
</tr>
</tbody>
</table>

(continued on the following page)
## High Speed Interface Macros

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>Process Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>90nm</td>
</tr>
<tr>
<td>Serial ATA</td>
<td>SATA3 AHCI</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>SATA2 AHCI</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SATA3 Device</td>
<td>✔️</td>
</tr>
<tr>
<td>DRAM Interface (PHY)</td>
<td>DDR3</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>DDR3L</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>DDR4</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>LPDDR3</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>LPDDR4</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>LPDDR4X</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>HBM2</td>
<td>✔️</td>
</tr>
</tbody>
</table>

## Analog Macros

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>Process Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>90nm</td>
</tr>
<tr>
<td>ADC</td>
<td>10bit, up to 600MS/s</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>12bit, up to 200MS/s</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>16bit</td>
<td>✔️</td>
</tr>
<tr>
<td>DAC</td>
<td>10bit, up to 220MS/s</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>12bit, up to 110MS/s</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>16bit</td>
<td>✔️</td>
</tr>
<tr>
<td>AFE</td>
<td>Audio</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Video</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Scanner</td>
<td>✔️</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>+/-5deg.C accuracy (without trimming)</td>
<td>✔️</td>
</tr>
<tr>
<td>Power management</td>
<td>Vin=3.3V, Vout=1.0-1.2V, Iout ≤400mA LDO</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Power on reset</td>
<td>✔️</td>
</tr>
<tr>
<td>Standard PLL</td>
<td>Fout: ~1200MHz, Fin:10–200MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~1600MHz, Fin:16–200MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~2400MHz, Fin:16–200MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~3200MHz, Fin:16–200MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~5000MHz, Fin:20–100MHz</td>
<td>✔️</td>
</tr>
<tr>
<td>Low Jitter PLL</td>
<td>Fout: ~600MHz, Fin:11–100MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~1000MHz, Fin:10–40MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~6400MHz, Fin:20–100MHz</td>
<td>✔️</td>
</tr>
<tr>
<td>Fractional -N PLL</td>
<td>Fout: ~1600MHz, Fin:10–50MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~2400MHz, Fin:10–50MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~3200MHz, Fin:10–50MHz</td>
<td>✔️</td>
</tr>
<tr>
<td>SSCG</td>
<td>Fout: ~1600MHz, Fin:10–50MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~2400MHz, Fin:20–50MHz</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Fout: ~3200MHz, Fin:10–50MHz</td>
<td>✔️</td>
</tr>
</tbody>
</table>
**Interface Macros**

**DDR Interface**

Socionext provides various DDR interface macros from low-to-middle speed forwarding bandwidth to high-speed forwarding bandwidth or low power, with various process technologies. Moreover, we support development for signal quality and cost optimization through design support by Chip-Package-Board co-design.

- **DDR interface macros**
  - High-speed/high-bandwidth DDR3/DDR4
  - Low power LPDDR4X/4/3/2 DDR3L
  - DFI compliant (all macro)
  - Compatible with many different DRAM configurations and PKG options, such as Fly-by, PoP, and DIMM thanks to the PHY function (training function).

- **DDR interface design support (Chip-Package-Board codesign)**
  - Timing verification: Verifies the timing of all DDR-IF systems including delays between LSI I/O and DRAM
  - Power Integrity: Optimizes the parasitic inductance, resonant frequency, and power supply (PKG, PCB) impedance as part of the power supply impedance design
  - Signal Integrity: Optimizes Driver strength, terminator resistance, and interconnect topology
  - Bus switching verifications: Optimizes the write and read bus switch timing

**Memory Controllers**

Socionext provides various memory solutions for system optimization. We also offer consulting services on memory systems including memory channels and the system bus to maximize SoC performance.

- **Memory controller IP**
  - Controller for maximizing high DRAM utilization

- **QoS-Arbiter IP**
  - High performance QoS-Arbiter featuring multiple functions

- **BusIP**
  - Original low power consumption bus with high layout flexibility

- **MonitorIP**
  - Visualizes memory system performance in real-time
  - Monitors performance (bandwidth, latency) and provides an environment for tuning parameters

**DDR Interface Configuration Diagram**

**LPDDR4-3733 DQ Waveforms**

**Bus Switching Waveforms**
MIPI Interface

This high-speed interface is used to build a camera and display system by combining high-speed, high resolution CMOS image sensors. This interface provides a solution for highly expressive images.

- MIPI D-PHY TX macro
  Small footprint, high-performance macro with the maximum speed of 4.5 Gbps
  - 4-data lane + 1-clock lane configuration
  - Transmission speed: 80 Mbps to 4.5 Gbps per lane
  - Equalization function
  - The world's smallest footprint
  - D-PHY2.0 compliant

PCI Express Interface

As a result of the recent rapid improvement in CPU processing capability and an increase in the need for high capacity data transfer, it has become extremely difficult to achieve the expected system performance with existing buses. The PCI Express technology is a high-speed interface capable of transferring several hundred megabytes of data that can overcome this issue.

Socionext's PCI Express macro supports up to 8 GT/s (Gen3) and passed the PCI Express standard compliance test hosted by the Peripheral Component Interconnect Special Interest Group (PCI-SIG), and its interconnectivity and reliability have been confirmed with many PCI Express interfaces.

- PCI Express LINK macro
  - Compliant with the PCI Express Base Specification rev.3.0 standard specification
  - Support for x1, x4, and x8 lanes
  - DualMode (RootComplex or Endpoint is selectable)
  - Possible to select AMBA3 I/F as the user interface
  - Built-in DMAC

- PCI Express PHY macro
  - Maximum transfer bit rate of 64 GT/s
  - High-speed signal transmission with the de-emphasis function is guaranteed
  - The LINK macro interface is compliant with the PIPE3 and PIPE4 standard specifications
10G-28Gbps SerDes Interface

With transmission performance of 10Gbps–28Gbps per channel and a configuration comprised of multiple channels, we provide a high-performance SerDes macro for constructing 100G/200G/400G optical networks or 100G Ether systems.

The built-in low-jitter, high-performance PLL enables robust transmission up to 28 Gbps per channel. It also supports various standards including OIF-CEI-11G-SR, OIF-CEI-28G-SR, OIF-CEI-28G-VSR, IEEE802.3ba CAUI, IEEE802.3bm CAUI4, XFI and so forth.

- ×1, ×4 lane configuration.
- Comprised of Transmitter/Receiver/PLL and capable of bidirectional communication with 1 macro.
- Up to 112.8 Gbps per macro (for unidirectional, ×4 configuration).
- Support for power-down control on each lane.
- Support for power-down control for the entire macro.
- Implementing Clock-Data Recovery for each Receiver lane.
- Transmitter Equalization supported.
- Receiver Equalization supported.
- Built-in termination resistor in Transmitter/Receiver.
- Organic flip chip package.

(0.8 mm/1.0 mm Ball Pitch, HDBU Package)
Analog Macros

We offer various analog macros (data converter, power management, temperature sensor, analog front-end) for our customers’ development to address various applications including communication, image processing, sensors and control.

• All macros are silicon verified.
• Implemented on many custom SoCs with a track record in mass production.

Data Converters

We offer various data converter macros addressing low power consumption and a small area which are demanded in SoCs.

• Pipeline & high speed SAR ADC
  • 10-bit/12-bit resolution, maximum 600MSPS conversion rates
  • The world’s smallest class power consumption

• ΔΣ ADC
  • Applicable to 16bit to 24bit resolutions
  • Power consumption of up to 1 mW with high precision SINAD 85 dB

• ΔΣ DAC
  • Applicable to 16bit to 24bit resolutions
  • SINAD 90 dB. Power consumption is 1 mW or less

Power Management

We offer various power management macros that enable single power supply development which is demanded in SoCs.

• LDO for low-noise power supply applications
  • Lineup of small-area versions such as the integrated I/O type
  • Safety protection functions such as short-circuit detection
  • Supports power supply to analog IPs such as ADC and PLL

• Power-ON reset
  • Customizable voltage-detection level and reset time
  • Supports brown-out reset
Sensors and Analog Front-End (AFE)

We offer a sensor macro for measuring temperature and voltage inside the chip and a low power-consumption AFE for processing signals from various external sensors.

Temperature sensor macro
- Can monitor temperature inside the chip at high resolution (0.125°C)
- Low power consumption and small area allow installation of multiple sensors on one chip
- Realizes temperature-dependent voltage and frequency control system

Scanner AFE
- Supports both CCD and CIS
- Includes gain and offset adjustment function
- Comes with 12-bit, 50 MS/s ADC
- Low power consumption (19 mW)

Custom AFE that supports various sensor signals and external signals
- AFE for optical sensor, humidity sensor, and gyro sensor
- Video AFE
- Audio AFE
- Digital TV AFE
Design Technology

Front-end Design

We offer a development environment using standard EDA tools as a SoC development environment for customers and a tool we created for improving design efficiency as a design kit. The front-end design kit, which is uniquely optimized by Socionext, enables the development of high performance, small chip size, low power LSIs.

EDA tools supported by Socionext front-end design kit

<table>
<thead>
<tr>
<th>High level synthesis</th>
<th>Catapult<em>1, C-to-Silicon Compiler</em>1, Stratus*1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTL style check</td>
<td>SpyGlass*2</td>
</tr>
<tr>
<td>Functional verification</td>
<td>Verilog-HDL, Incisive Enterprise Simulator<em>1, Questa</em>2, VCS-MX, VCS*2</td>
</tr>
<tr>
<td>VHDLL</td>
<td>Incisive Enterprise Simulator<em>1, Questa</em>2, VCS-MX*2</td>
</tr>
<tr>
<td>CPF/UPF</td>
<td>Incisive Enterprise Simulator-XL<em>2, Questa</em>3, VCS-NLP*2</td>
</tr>
<tr>
<td>Logic synthesis</td>
<td>Design Compiler<em>2, Encounter RTL Compiler</em>1, Genus Synthesis Solution*1</td>
</tr>
<tr>
<td>Equivalence verification</td>
<td>Encounter Conformal Equivalence Checker<em>1, Formality</em>2</td>
</tr>
<tr>
<td>Timing constraint verification</td>
<td>Encounter Conformal Constraint Designer<em>1, SpyGlass Constraints</em>2</td>
</tr>
<tr>
<td>MV verification</td>
<td>Encounter Conformal Lowpower<em>1, VC Static Low Power</em>2</td>
</tr>
<tr>
<td>Analysis/debugger</td>
<td>Verdi*2</td>
</tr>
<tr>
<td>Netlist check*</td>
<td>SpyGlass*2</td>
</tr>
<tr>
<td>Pre-DFT check*</td>
<td>SpyGlass DFT*2</td>
</tr>
</tbody>
</table>

*1: Cadence, Inc.  
*2: Synopsys, Inc.  
*3: Mentor Graphics Co.  
* : We provide a checker we developed in-house to suit the technology.

Design specification I/F

Designing an SoC requires not only RTL and netlist as logic design data, but the power intent, such as the SDC describing timing specifications including clock frequency, and CPF/UPF containing power supply specifications, including power gating design and multi-power/multi-voltage design. We provide interface files in our unique format for such SDC and power intent. Using such files allows you to improve efficiency in writing and reviewing specifications and quickly verify the consistency between the handed-off RTL, power supply specifications, and timing specifications as well as layout compatibility.

Physical aware logic synthesis

Due to progress in technology, logic design that takes layout into account is becoming important for improving SoC design efficiency as well as optimizing area and timing. For this reason, we adopt physical aware synthesis that performs optimization by taking the actual layout into account. Through this co-design between the logic design and layout design, we can efficiently design sophisticated SoCs for your product.
Low Power Design Solutions

The demand for reducing the power consumption of LSIs has been getting stronger in recent years. In our SoC design efforts, we are undertaking various initiatives to meet customers' demands for lower power consumption. In order to achieve low power consumption LSIs, it is effective to combine various kinds of technologies as well as using individual technologies. Socionext’s design environment “Reference Design Flow” supports various low power consumption technologies and enables the power consumption of LSIs to be reduced during both operation and standby. By controlling the power supply in particular, we develop methodologies for systematically achieving low power consumption. Also, by fully adopting UPF/CPF, we make low power consumption design, easy for customers while minimizing changes to their design assets. The use of UPF/CPF allows for high reliability designs even with low power consumption technology, which it has been extremely difficult to verify in the past.

● Multi voltage design

With this technology, different voltages are supplied to an LSI to reduce power consumption during the operation of circuit blocks for a high-speed operation circuit block, a high voltage is supplied, and for a low-speed operation circuit block, a low voltage is supplied. Using UPF/CPF allows physical design and verification of circuit blocks with different voltages to be performed together, minimizing extension of the development period for low power consumption design.

● Clock gating

Clock gating enables the power consumption of LSIs during operation to be reduced by stopping the supply of clock signals to circuit blocks that do not need to operate.

● Power management

We provide power management technology to control power gating, SRAM sleep, and shut-down mode in a comprehensive manner. By thoroughly eliminating useless, this technology contributes to low power consumption. With its unique power switch controlling system, Socionext’s power management technology suppresses the rush current noise generated when the power supply is turned on and off to prevent LSIs from malfunctioning. In addition, using UPF/CPF allows physical design and verification of circuit blocks that have a power shutdown circuit to be performed together, minimizing extension of the development period.

● Adaptive power supply control (DVFS*, AVS*/Advanced-AVS)

We can use DVFS, which is for varying the voltage and frequency according to the required throughput.
Custom SoC

This technology also adaptively determines the operating voltage according to voltage variation due to manufacturing variability and operates the LSI at the lowest voltage at which its operation is guaranteed, leading to reduced power consumption of the LSI during both operation and standby.

*: DVFS (Dynamic Voltage Frequency Scaling)
**: AVS (Adaptive Voltage Scaling)

Standard cell

In the area of advanced technology, in addition to the standard cell area, routability contributes to the low power consumption of LSIs. We provide our original standard cell that is far superior to that of other companies. In addition, we offer a rich line-up of cells that are effective for achieving low power consumption of the clock system.

Low power SRAM

An LSI with high-capacity SRAM may have a problem with the power consumption of the SRAM macro. In such cases, power consumption may be reduced by using a multi-mode SRAM. Multi-mode SRAM features a standby mode, sleep mode, and shut-down mode, as well as a normal operation mode. The standby mode allows for the operating power of an SRAM macro to be 0 by stopping the clock operation inside the macro. In sleep mode, leakage power is reduced by deactivating peripheral circuits of the SRAM macro. Power can only be shut down with an SRAM in shutdown mode. The optimization of the SRAM configuration to be used contributes to low power consumption as well. We help customers select the best SRAM from the logic design phase.

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Function</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>To operate RAM normally</td>
<td>--</td>
</tr>
<tr>
<td>Standby</td>
<td>To stop the SRAM operation</td>
<td>The operating power is 0</td>
</tr>
<tr>
<td>Sleep</td>
<td>To retain data</td>
<td>Leakage power is reduced to one-third**</td>
</tr>
<tr>
<td>Shutdown</td>
<td>To shut down the power with only the SRAM</td>
<td>Leakage power is reduced to one-sixth**</td>
</tr>
</tbody>
</table>

*: Depends on the SRAM structure

Low power design environment that fully adopts UPF/CPF

Socionext offers a total solution that supports power gating, multi power supply, and multi-voltage design through consistent power supply specification management with UPF*1 and CPF*2. RTL simulation for complicated power supply design due to an increased number of integrated IPs, multi power supply verification, and physical design. This solution allows power shutdown verification to be performed based on RTL simulation by managing power supply specifications as separate logical and physical specifications and defining only the logical specification. Verified RTL and the logical specification for the power supply are handed off to physical design, the power supply physical specification that defines the power supply connection is prepared, and then physical design is performed based on these power supply specifications (UPF/CPF). Managing the power supply specification with UPF/CPF in this way and using it through a design flow clarifies the power supply specification and allows for high reliability design.

*: UPF (Unified Power Format) is a standard specification that defines the Low power design guidelines standardized as IEEE Std. 1801. (http://www.ieee.org/)
**: CPF (Common Power Format) is a standard specification that defines the Low power design guidelines standardized as Si2. (http://www.si2.org/?page=811)
SoC testing is becoming more complicated as processes become more refined, circuit scale increases, circuit operation becomes faster, and much less power is consumed. To resolve this issue, in addition to compressed scan, memory BIST, and boundary scan DFT, we perform high quality testing using various types of DFT technology for improved test quality and yield.

[DFT Technologies Adopted by Socionext]
- At-speed and low power test technologies for improved test quality
  - Test using on-chip PLL clocks
  - Test that controls power consumption during testing
- Memory redundancy repair process and fault diagnosis technologies for improved yield
We layout customer design with our high-accuracy analysis technology, high performance synthesis, placement, routing, and high speed technology, and low noise design technology.

**Physical aware logic synthesis**

Due to the increase in circuit size and routing load caused by the progress of refinement, the gap between the estimate at the time of logic synthesis and layout is widening. At Socionext, we minimize the gap with the layout by taking into account layout information from the logic synthesis step. This allows for early confirmation of timing convergence, thereby shortening the development period.

**UPF and CPF support**

We support UPF and CPF and perform physical design and physical verification based on power supply specifications for which functional verification is conducted. This enables high design quality to be achieved even for complex low power consumption technologies.

**Multiple mode/corner-aware optimization**

As refinement progresses, the processes, voltage, and temperature conditions (corner conditions) that should be taken into account are increasing. In addition, the number of operation modes is increasing to enhance multifunctionality and secure the reliability of LSIs. In our physical design, placement, routing, and optimization that take into account multiple corner conditions and operation modes are performed. This makes it possible to reduce the iteration of timing optimization due to conflicts between different corners and modes, which shortens the development period.

**Power rail analysis/crosstalk noise analysis**

As refinement progresses and voltages become lower, the delay variation due to an IR drop (voltage drop) in LSIs and crosstalk noise increases. Through high accuracy IR drop and crosstalk noise analysis, we have verified that they do not affect system operations.
Socionext achieves perfect operation on the first attempt through LSI development based on the chip, package, and PCB codesign flow. While offering a good forecast for design through reference design, we develop and improve LSI models (IBIS, timing model, LSI power supply model) necessary for transmission line analysis of DDR4 and other memory interfaces and USB3.0 and other SerDes interfaces to achieve total optimization in each phase of design based on integrated chips, packages, and PCB analysis. This allows for an issue that used to only be discovered in the actual design phase to be addressed in the prototyping phase.

We offer customers IBIS and a timing model early on in the design stage so that they can conduct transmission line analysis taking timing into account.

The use of IBIS5.0 and an LSI power supply model (chip and package) for PCB power supply impedance analysis and SSO noise analysis allows customers to perform high accuracy development in a short TAT.

**Chips designed with noise in mind, packages, and PCB co-design**

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We offer customers IBIS and a timing model early on in the design stage so that they can conduct transmission line analysis taking timing into account.
Simulation

Utilizing advanced simulation technologies, we offer the best package solution.

Mechanism simulation
Incorporating mechanism simulation into package design allows customers to propose high reliability packages.

Thermal design simulation
By combining actual measurement of thermal resistors and thermofluid simulation, we perform high accuracy thermal resistance analysis reproducing the operating environment of products.

Thermal resistance measurements
Measurement of transient thermal resistance values in accordance with the JEDEC standard JESD51-14 is possible.
Manufacturing Technology Package

Technologies and Device Products

Our device products from 90 nm to 12 nm include standard cell types supporting a wide range of technologies. Socionext is working with multiple foundry partners. Thanks to the synergy effect of their manufacturing capability and the quality control system and design engineering ability of Socionext, we will continue to lead the LSI industry in design and manufacture of cutting-edge custom SoCs.

● Standard cell

<table>
<thead>
<tr>
<th>Technology</th>
<th>Device Product Name</th>
<th>Power Supply Voltage (Typ.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 nm FinFET CMOS</td>
<td>T.B.D.</td>
<td>T.B.D</td>
</tr>
<tr>
<td>12 nm FinFET CMOS</td>
<td>CS661 series</td>
<td>+0.7V ±0.07V / +0.8V ±0.08V</td>
</tr>
<tr>
<td>16 nm FinFET CMOS</td>
<td>CS602 series</td>
<td>+0.7V ±0.07V / +0.8V ±0.08V</td>
</tr>
<tr>
<td>28 nm Metal Gate CMOS</td>
<td>CS407 series</td>
<td>+0.8V ±0.08V / +0.9V ±0.09V</td>
</tr>
<tr>
<td>28 nm Metal Gate CMOS</td>
<td>CS405 series</td>
<td>+0.9V ±0.09V</td>
</tr>
<tr>
<td>40 nm Si Gate CMOS</td>
<td>CS302 series</td>
<td>+1.1V ±0.1V</td>
</tr>
<tr>
<td>55 nm Si Gate CMOS</td>
<td>CS251 series</td>
<td>+1.2V ±0.1V</td>
</tr>
<tr>
<td>65 nm Si Gate CMOS</td>
<td>CS201 series</td>
<td>+0.9 V to +1.3 V (supports a wide range)</td>
</tr>
<tr>
<td>90 nm Si Gate CMOS</td>
<td>CS101 series</td>
<td>+0.9 V to +1.3 V (supports a wide range)</td>
</tr>
</tbody>
</table>

● Gate scale comparison

- 12nm CS661
- 16nm CS602
- 28nm CS405/CS407
- 40nm CS302
- 55nm CS251
- 65nm CS201
- 90nm CS101

● Power consumption comparison

*1 : The vertical axis shows the relative ratio of each technology using the total power (sum of the dynamic component and leakage component) of CS101 as the criterion.
Advanced Packages

Package System

From high performance models for high end use to high cost performance models for consumer use, we provide a wide range of packages.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Package Structure</th>
<th>Thermal Resistor $\Theta_{ja}$ ($^\circ$C/W)</th>
<th>Example Purposes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC-CBGA</td>
<td></td>
<td>7~</td>
<td>Servers, high-speed large capacity network, etc.</td>
</tr>
<tr>
<td>FC-PBGA</td>
<td></td>
<td>7~</td>
<td>Factory automation, office equipment, medical care, health care, satellite broadcasting, digital TVs, set-top boxes, digital signage, etc.</td>
</tr>
<tr>
<td>(Low loss tan$\delta$BU)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FC-PBGA (Conventional)</td>
<td></td>
<td>9~</td>
<td></td>
</tr>
<tr>
<td>TEBGA</td>
<td></td>
<td>13~</td>
<td>Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.</td>
</tr>
<tr>
<td>PBGA</td>
<td></td>
<td>15~</td>
<td></td>
</tr>
<tr>
<td>FBGA</td>
<td></td>
<td>17~ to 60</td>
<td>Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.</td>
</tr>
<tr>
<td>FCCSP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QFN</td>
<td></td>
<td>20~ to 40</td>
<td></td>
</tr>
<tr>
<td>WL-CSP</td>
<td></td>
<td>25~ to 60</td>
<td></td>
</tr>
<tr>
<td>LQFP/TEQFP</td>
<td></td>
<td>15~ to 100</td>
<td></td>
</tr>
</tbody>
</table>

*1: Reference value. The thermal resistance value varies depending on the chip size or package specification. Inquire to us regarding individual cases.

Package Roadmap

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