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Data Sheet

MB88F334
MB88F336

Rev1.20 | June 30, 2020

Socionext Europe GmbH

Graphic Competence Center – GCC

Attached Files

Preface

Purpose of this Document

This document describes and gives you detailed insight to the stated Socionext Europe GmbH product.

The MB88F334 and MB88F336 devices belong to the Indigo Family used for graphics applications.

This document is intended for engineers developing products which will use the MB88F334 and MB88F336 devices. It describes the function and operation of the devices. Please read this document carefully.

Trademarks

APIX is a registered trademark of Inova Semiconductors GmbH, Munich, Germany.

ARM is a registered trademark of ARM Limited in UK, USA and Taiwan.

ARM is a trademark of ARM Limited in Japan and Korea.

System names and product names which appear in this document are the trademarks of the respective company or organization.

Licenses

Under the conditions of Philips corporation I2C patent, the license is valid where the device is used in an I2C system which conforms to the I2C standard specification by Philips Corporation.

The purchase of a Socionext I2C components conveys a license under the Philips I2C Patent Rights to use these components in an I2C system, provided that the system conforms to the I2C Standard Specification as defined by Philips.

Contact Us

For more information on Socionext products as well as support and sales inquiries, please visit us at www.eu.socionext.com.

History

Revision	Date	Author	Description
0.01	05.04.2012	RvR	First draft (short version)
0.02	02.05.2012	RvR	Features updated. Number of ADC channels updated. Pinning Description table updated. Absolute Maximum Ratings added. Thermal Design Consideration added. Power Consumption table added.
0.03	03.07.2012	RvR	Pinning Overview updated. Pinning Descriptions added. Chapters 2, 3, 4, 5, and 6 added. Chapter 7 updated.
0.04	18.07.2012	RvR	Pinning changes: Pin 10 and 16 (exchanged). Pin 10 description changed. Pin Multiplexing- Section Display Output added.
1.00	22.09.2017	ML	Set in Socionext format. Updated with information of MB88F334 MB88F336 Hardware Manual Rev.1-41.
1.01	17.05.2018	ML	Updated Table 2.7, “AC Timing Host-SPI Interface” Added “1.3. Device Comparison” Corrected formatting issues.
1.10	08.11.2018	ML	Updated “1.4. Block Diagram”.
1.15	18.07.2019	ML	Updated “Warranty and Disclaimer”.
1.20	30.06.2020	ML	Updated Figure 2.14, “ADC input signal” in chapter “2.10. ADC”. Added document security classification.

Table of Contents

1. Introduction

Note: Please check the “History” page for a record of changes made to the last version.

1.1. General

The MB88F334 and MB88F336 belong to the Indigo family of graphics controllers designed for remote display applications in the automotive industry. They are optimized to work together with our MB86R12, MB86R91, and the INAP37x from Inova Semiconductors GmbH to control a dashboard display, Head-up-Display (HUD) systems and a Central Information Display (CID). In addition, the MB88F334 and MB88F336 display controllers can be used to enable APIX2 (APIX version 2.0) based display systems in multiple applications in the automotive and industrial market segments.

The differences between the MB88F33X family devices are documented here. The differences can be summarized as follows:

- MB88F334: The main, fully-featured device.
- MB88F336: As the MB88F334 device, but without HDCP functionality at the APIX link.

1.2. Features

- Technology
  - CMOS 90nm (CU100F)
  - Power Supply Voltages:
    3.3 V → I/O Display Interface
    5.0 V (or 3.3 V) → I/O Peripherals
    5.0 V → Stepper motor
    1.2 V → Internal
- Package
  - QFP208
  - Ambient temperature range: -40°C...+105°C
- System Features
  - 160 MHz System Clock
  - Embedded flash Memory with ECC
    - 32kB
  - Embedded SRAM
    - 64kB
  - CPU/MCU/HOST Interface: Synchronous Serial Peripheral Interface (SPI), Automotive shell (AShell) sideband communication/link
  - Command Sequencer
  - DMA controller
  - Touch controller support (hardware accelerated communication with external touch devices)
  - Configuration FIFO (to de-couple host command stream and generate isochronous reconfiguration with internal peripherals)
  - High-Speed (quad) mode SPI for connection to external SPI flash
  - Spread spectrum clock modulation
  - Watchdog, alive sender, low voltage detection

- CRC checksum calculation for memory content

- APIX2 features
  - RX interface
    - Up to 3 GBit/s
    - APIX1 mode compatible
    - HDCP for video link (only MB88F334)
  - Daisy chain output, i.e., connect through of the high-speed downstream APIX signal from the RX input to an additional APIX compatible TX interface, as well as the APIX upstream channel in the other direction.
  - Sideband link
    - AShell Remote Handler
    - MII Interface/Ethernet over APIX
    - I2S output
- Graphics features
  - Integrated Pixel Engine (as opposed to Sprite Engine in the other Indigo Family devices)
  - Maximum pixel frequencies supported up to 144MHz (e.g. 1600x600 @100Hz, 1920x768 @60Hz)
  - Display of run length encoded (RLE) background image (on-the-fly decoding)
  - Display of icons with 1, 2, 4, 8bpp (indirect, i.e., color palette) or 16bpp, 24bpp (direct) color depth. Icon size up to 2048x2048 pixels, depending on internal memory available.
  - Icon on top of APIX video stream or on top of run length encoded background
  - Flicker-free/seamless switch between an APIX video stream and a background video stream
  - Dither and gamma unit
  - Four signature units, each can compute a value for a display output frame to be compared against a pre-computed reference in order to detect corrupted data.
  - Connection to displays with
    - RSDS interface using a TCON with single or dual 18 bpp or 24 bpp mode
    - TTL interface with single 18 bpp or 24 bpp mode (support of data inversion for low EMI) or
    - LVDS/OpenLDI single mode (24bit or 18bit per pixel, balanced or unbalanced) up to 75MHz pixel frequency
    - LVDS/OpenLDI dual mode (2x24bit or 2x18bit per pixel, balanced or unbalanced) up to 144MHz pixel frequency
- Peripherals
  - 6x stepper motor controllers
  - 16 channel ADC + 12 for Zero Point Detection (ZPD)
  - 2x I^2C
  - 1x USART or 1x LIN
  - SPI interface for up to 4 target devices (only one can be simultaneously served)
  - Sound capability I2S via APIX
  - Internal sound generator
  - 16 x PWMs (Pulse Width Modulation)
  - Max. 110 GPIOs (General Purpose I/Os). This is the maximum count when all I/O pins are switched to GPIO functionality.
  - 8x External Interrupts

1.3. Device Comparison

Table 1.1. : Indigo2 Family Device Comparison

	MB88F334	MB88F336	SC1711AH5
Chip Package			
Package, Pins	LQFP-208		EP-LQFP-176
Size, Pitch	28x28mm, 0.5mm		20x20mm, 0.4mm
Temperature Range	Ta -40 … +105°C		Ta -40 … +105°C
Memory			
Embedded SRAM	64kB		128kB
Embedded Flash	32kB		56kB
Graphics, Display Features			
2D Core	Socionext SEERIS - MVL		Socionext SEERIS - MVL
Video channels	2		1
Video Output Resolution	1920x1080@60Hz (18bit RGB) 1920x768@60Hz (24bit RGB)		1280x480@60Hz (24bit RGB)
Video Output	TCON-RSDS; TTL dual LVDS (OpenLDI)		TCON-RSDS; TTL dual LVDS (OpenLDI)
Video Formats, Decompression	RGBA, Indexed, Grey Scale, @ 8 bits per component		RGBA, Indexed, Grey Scale, @ 8 bits per component
Pixel Speed	144MHz		144MHz
Signature Units	4		4
Image Processing	CLUT, Matrix, Dither, Gamma, Sprites, α blending		CLUT, Matrix, Dither, Gamma, Sprites, α blending
Audio	I²S over APIX®2, Sound Generator		I²S over APIX®2, Sound Generator
APIX Down-/Up-stream	APIX®2 @ 3Gbps / 187 Mbps		APIX®2 @ 1Gbps / 187 Mbps
Content Protection	HDCP 1.4	-	-
Daisy Chain	Yes		No
Network	MII - Ethernet over APIX®2 @ 100 Mbps		MII - Ethernet over APIX®2 @ 100 Mbps
Core Clock	160MHz		160MHz
Peripherals			
Standard I/O	USART-LIN, I²C, GPIO, PWM, ADC, HS-SPI		USART-LIN, I²C, GPIO, PWM, ADC, HS-SPI
Stepper Motor Controllers	6		6

1.4. Block Diagram

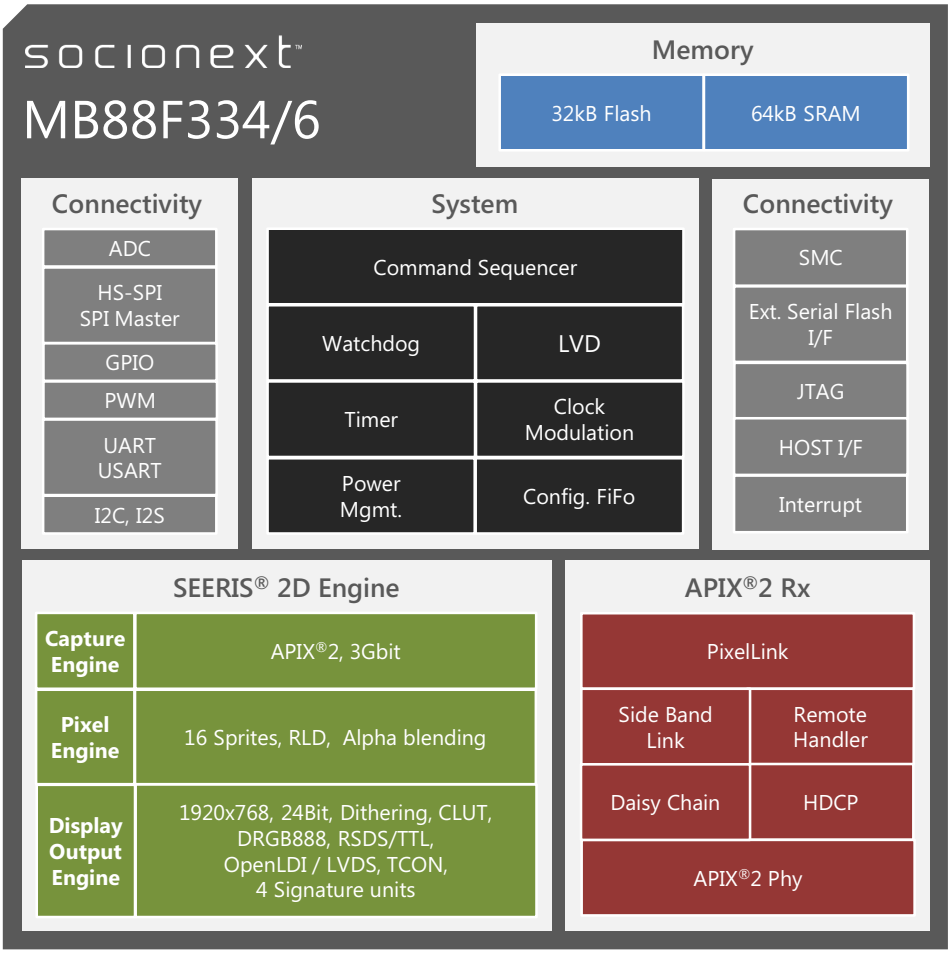


Figure 1.1. : Block diagram of MB88F334 / MB88F336

1.5. Part Number Code

The following diagram explain the meaning of the part number.

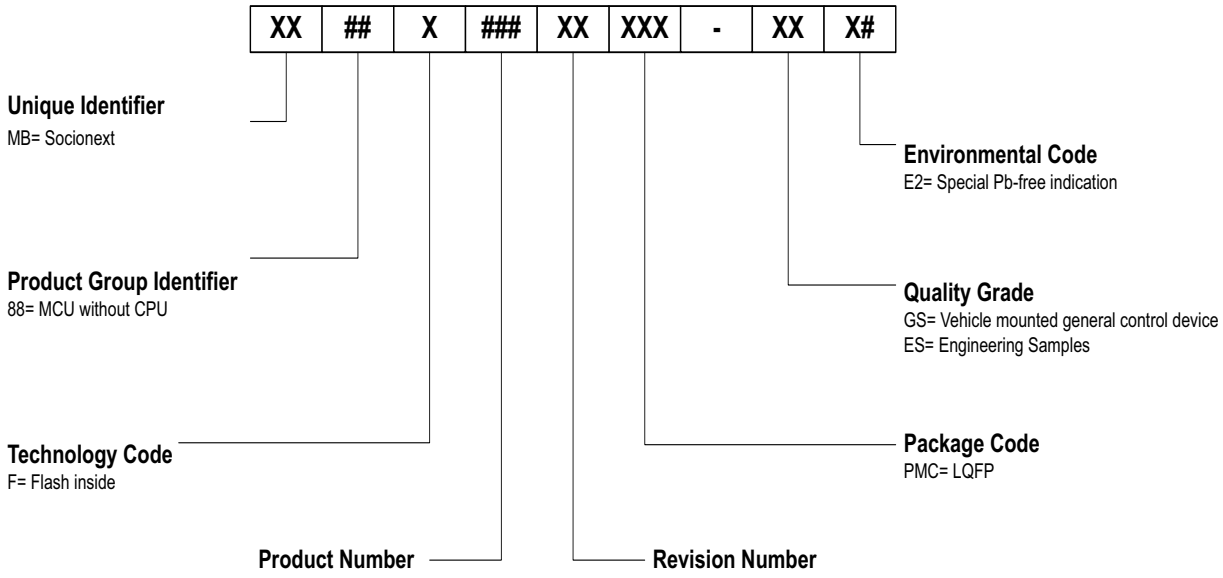


Figure 1.2. : Part Number Code

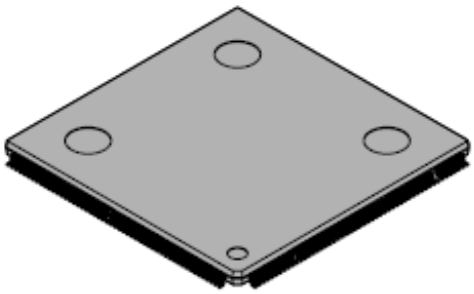
1.6. Ordering Numbers

Table 1.2. : Ordering Numbers

Part Number	Status	Description
MB88F334PMC-GSE2	Production Sample	The main, fully-featured device
MB88F336PMC-GSE2	Production Sample	As the MB88F334 device, but without HDCP functionality at the APIX link.

1.7. Package

FPT-208P-M06

208-pin plastic LQFP		
 (FPT-208P-M06)	Lead pitch	0.50 mm
	Package width × package length	28.0 × 28.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	2.55g
	Code (Reference)	P-LFQFP208-28×28-0.50

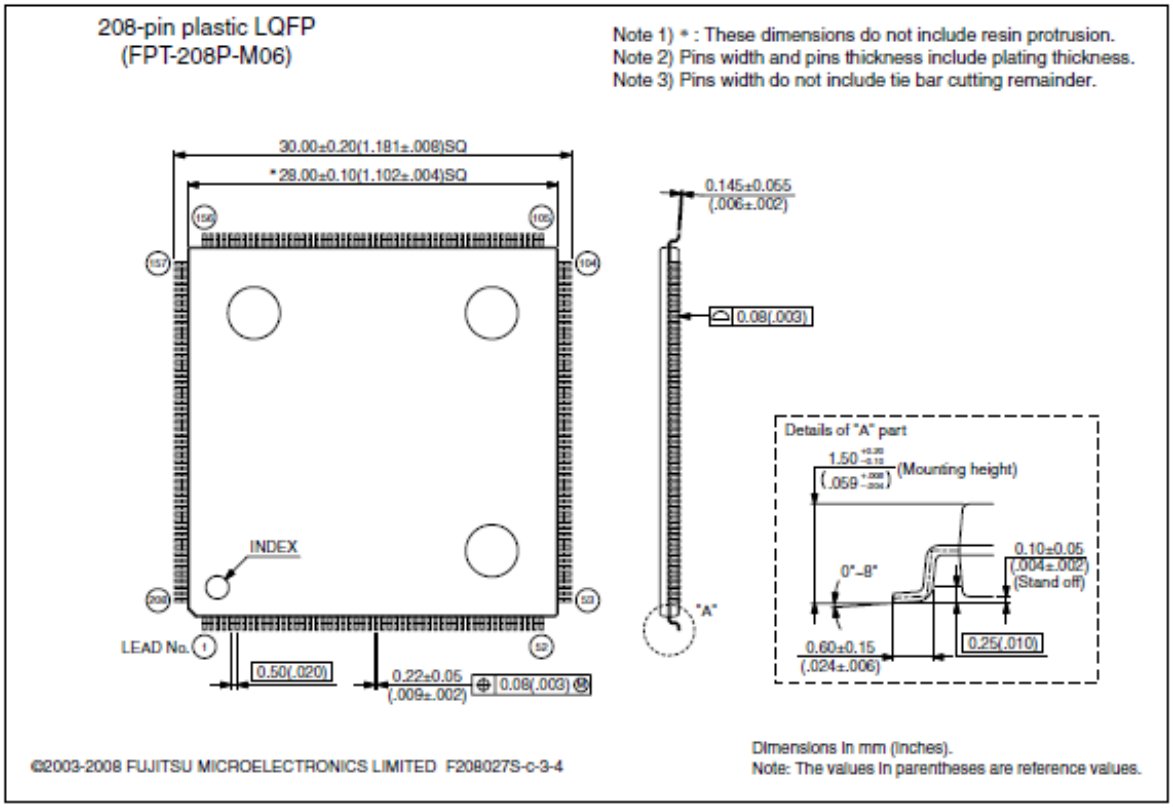


Figure 1.3. : FPT-208P-M06

1.8. Pinning

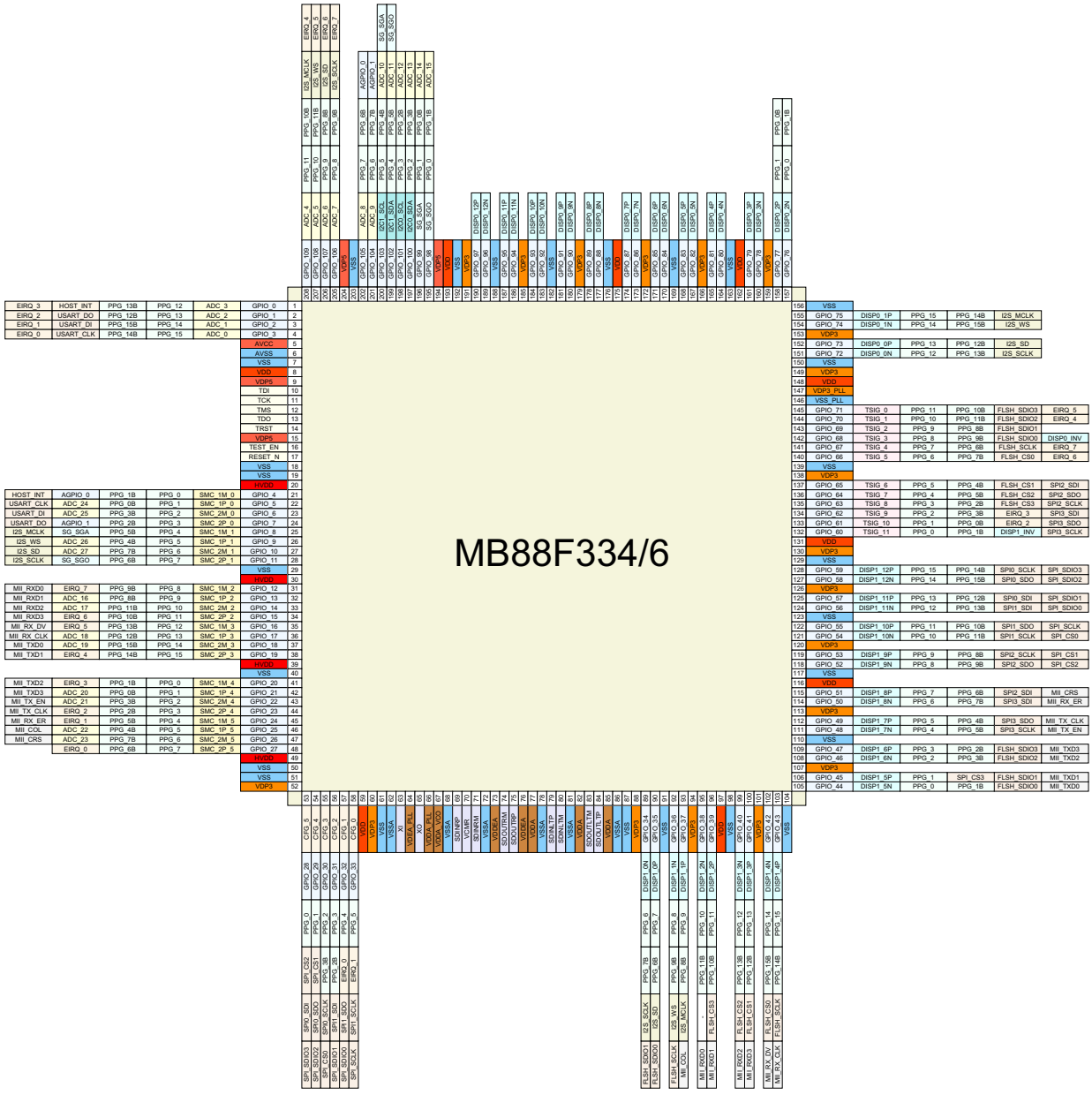


Figure 1.4. : Pinning Overview (showing multiplex functionality)

Note: If you are already familiar with Socionext GDCs and SoCs, you may associate the names DISP0... and DISP1... etc. with the control of multiple external displays (this was the naming convention used in previous documentation). However, the MB88F334 / MB88F336 devices can only be connected to a SINGLE external display panel. The names DISP0..., DISP1... etc. refer to the data channels used for the various physical connections (TTL, RSDS, LVDS) to a single panel.

1.8.1. Pin Descriptions

For detailed information please refer to the attached pin list "Pinning.xlsx".

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Table 2.1. : Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Comment
Core supply	VDD	VSS – 0.3	VSS + 1.8	V	
Display supply	VDP3	VSS – 0.3	VSS + 4.0	V	
Stepper supply	HVDD	VSS – 0.3	VSS + 6.0	V	≥ VDP5
GPIO supply	VDP5	VSS – 0.3	VSS + 6.0	V	≥ VDP3
ADC supply	AVCC	VSS – 0.3	VSS + 6.0	V	= VDP5
APIX supply	VDDA VDDA_VCO VDDA_PLL VDDEA VDEA_PLL	VSS – 0.3 VSS – 0.3 VSS – 0.3 VSS – 0.3 VSS – 0.3	VSS + 1.8 VSS + 1.8 VSS + 1.8 VSS + 4.0 VSS + 4.0	V V V V V	
Input voltage	VI	VSS – 0.3 VSS – 0.3 VSS – 0.3	VDP5 + 0.3 VDP3 + 0.3 HVDD + 0.3	V V V	< 6.0 V < 4.0 V < 6.0 V
Analog input voltage	VIA	VSS – 0.3	AVCC + 0.3	V	< 6.0 V
APIX analog Input Voltage	VIAPX	VSS – 0.3	VDDEA + 0.3	V	< 4.0 V, SD-OUT, SDIN, VCM
Output voltage	VO	VSS – 0.3 VSS – 0.3 VSS – 0.3	VDP5 + 0.3 VDP3 + 0.3 HVDD + 0.3	V V V	< 6.0 V < 4.0 V < 6.0 V
Storage temperature	T_{ST}	-55	150	°C	

Note:

- Applying stress exceeding the maximum ratings (voltage, current, temperature, etc.) may cause damage to semiconductor devices. Never exceed the ratings above.
- Never connect IC outputs or I/O pins directly, or connect them to VDD or VSS directly; otherwise thermal destruction of elements will result, but which does not apply to pins designed to prevent signal collision.
- Provide ESD protection, such as grounding when handling the product; otherwise externally-charged electric charge flows inside the IC and discharges, which may result in damage to the circuit.
- Applying voltage higher than VDD or lower than VSS to I/O pins of CMOS IC, or applying voltage higher than the ratings between VDD and VSS may cause latch up. The latch up increases supply current, resulting in thermal destruction of elements. When handling the product, never exceed the maximum ratings.

2.2. Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are guaranteed when the device is operated within these ranges. Semiconductor devices must always be operated within their recommended operating condition ranges. Operating outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented in the data sheet. Users considering application fields beyond the listed conditions are advised to contact their Socionext representatives beforehand.

Table 2.2. : Operating Conditions

Parameter	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Core supply	VDD	1.1	1.2	1.3	V	
Display supply	VDP3 VDP3_PLL	3.0 3.0	3.3 3.3	3.6 3.6	V V	
Stepper supply	HVDD	4.5 3.0	5.0 3.3	5.5 3.6	V V	≥ VDP5
GPIO supply	VDP5	4.5 3.0	5.0 3.3	5.5 3.6	V V	≥ VDP3, only for IO usage
ADC supply	AVCC	4.5 3.0	5.0 3.3	5.5 3.6	V V	= VDP5
APIX supply	VDDA VDDA_VCO VDDA_PLL VDDEA VDEA_PLL	1.1 1.1 1.1 3.0 3.0	1.2 1.2 1.2 3.3 3.3	1.30 1.30 1.30 3.6 3.6	V V V V V	
Junction temperature	T*j*	-40		135	C	
Ambient temperature	Ta *1	-40		105	°C	$R_{th\text{-}ja}$ = 34K/W (no airflow) Under JEDEC standard JESD51-2 conditions.
Case temperature	Tc *1	-40		115	°C	
*1 Note: Both operating conditions, Ta and Tc, have to be fulfilled. Please refer to section “2.3.5. Thermal Design Considerations”						

2.2.1. Supply Modes

Three supply modes are supported for MB88F334, and MB88F336.

Table 2.3. : Supply Operational modes

VDP5	AVCC	HVDD	Comment
5.0V	5.0V	5.0V	
3.3V	3.3V	5.0V	no ZPD
3.3V	3.3V	3.3V	no Stepper

WARNING:

AVCC and VDP5 must be set to the same voltage. It is required that AVCC does not exceed VDP5 and that the voltage at the analog inputs does not exceed AVCC neither when the power is switched on.

HVDD, AVCC and VDP5 must be set to the same voltage during zero point detection (ZPD) on any of the SMC ports. If zero point detection is not required on any of the SMC ports, then VDP5 and AVCC can have any value which is equal or lower HVDD.

2.3. Power Consumption

Table 2.4. : Supply currents

Parameter	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Core supply Note 1)	I_{VDD}			350	mA	
Display supply Note 2)	I_{VDP3} I_{VDP3_PLL}			80 170 100 200 40 80 10	mA mA mA mA mA mA mA	Single TTL @40 MHz Single TTL @85 MHz Single RSDS Dual RSDS Single LVDS Dual LVDS
Stepper supply Note 3)	I_{HVDD}			720	mA	max. 30 mA per pin
GPIO supply	I_{VDP5}			20	mA	
ADC supply	I_{AVCC}			5.0	mA	
APIX supply Note 4)	I_{VDDA} I_{VDDA_VCO} I_{VDDA_PLL} I_{VDDEA} I_{VDEA_PLL}			55 100 8.0 8.0 20 50 8.0	mA mA mA mA mA mA mA	Daisy chain disabled Daisy chain enabled Daisy chain disabled Daisy chain enabled

1) See “VDD Supply Current (Note 1)” below
2) See “Display IO Supply Current (Note 2)” below
3) See “Stepper IO Supply Current (Note 3)” below
4) See “APIX Supply Current (Note 4)” below

2.3.1. VDD Supply Current (Note 1)

The core supply current (I_{VDD}) mainly depend on the supply voltage, the chip temperature, and the internal frequencies. The given number is for maximum supply (1.3V), maximum temperature (105°C), and maximum internal frequencies. The following table give some more values, which allows a estimation for different use cases.

Table 2.5. : Core supply currents

Operation mode	Ta_{max} =105°C		Ta_{max}=85°C	
	1.3V	1.2V	1.3V	1.2V
"axi_clk = 160MHz, peri_clk = 80MHz, pixel clock = 144MHz"	350mA	310mA	340mA	300mA
"axi_clk = 80MHz, peri_clk = 80MHz, pixel clock = 40MHz"	240mA	210mA	230mA	200mA

Internal clocks should be setup as low as possible for low power consumption. All clock divider can be reprogrammed during operation. So, it is for example possible to increase and decrease the AHB clock divider for short phases of high speed operations. The video clock frequencies depends on the selected display and define

the internal pixel clock frequency. The minimum required axi_clk frequency can be estimated from the selected pixel frequency of the display. For standard setups the axi_clk should be set to be 10% to 30% higher than the pixel clock frequency.

The minimum required peri_clk frequency depends on the selected peripherals with their speed requirements.In addition, the core power consumption can be decreased by up to 10%, when disabling unused functions with the register PWR_CTRL.

2.3.2. Display IO Supply Current (Note 2)

For the estimation of the supply current I_{VDP3} the next rules can be followed:

- For every enabled differential pad the current rises by 7.5mA. For example, if 13 differential pads are enabled, it will consume 13 * 7.5mA = 97.5mA. This current is independent of the supply voltage or chip temperature.
- For all pins, when used as a CMOS output, the maximum current depends on the supply voltage, on the toggle rate, and the load capacitance. The current scales nearly linear with these parameters.
- The values in the table for the TTL panels give the maximum value for high supply voltage (3.6V), when using a ‘state-of-the-art’ TTL 24-bit panel connected though a ribbon cable with a realistic video content. Different systems may require more or less current.

2.3.3. Stepper IO Supply Current (Note 3)

The maximum current value in the table is the maximum current which MB88F334 / MB88F336 can deliver. For a stepper application, where the stepper is controlled by a sinusoidal way, the current for the 4 pins connected to one stepper can be estimated as:

$$\text{Current\_for\_one\_stepper} = 4 \times \frac{1}{\sqrt{2}} \times \text{Current\_for\_one\_pin}$$

For power dissipation, one has to use the VOL and VOH of the IO cells. The maximum value for both is 0.5V. The power than is estimated as:

$$\text{Power\_for\_one\_stepper} = 0.5V \times \text{Current\_for\_one\_stepper}$$

2.3.4. APIX Supply Current (Note 4)

The supply currents for the APIX are independent of the operation mode. There are two main influences for this currents.

First, if daisy chain is enabled or disabled (see values in the table).

Second, the selected drive strength for the transmitter outputs. This influences the I_{VDDEA} current. The values in the table give the maximum possible current.

For low power it should be ensure, that the daisy chain part of the APIX PHY is in power down when not needed (register PHY_PWR_CTRL.en_lt = 0). In addition, the drive strength should be set to the minimum setting that is required for the application (register PHY_RX_TST.rx_upstream_swing).

2.3.5. Thermal Design Considerations

The maximum permissible case temperature (T_C) is 115C. To ensure the device's reliability and its proper operation, do not exceed this temperature.

Note: MB88F334 / MB88F336 is not the only contributor to the thermal performance of the entire system. The PCB characteristics and layout, as well as the ambient temperature must also be taken into consideration to comply with the maximum case temperature restriction.

The estimated case-to-ambient thermal resistance (θ_{CA}) is 28 K/W for a 4-layer PCB with no air flow and no heat sink. This thermal performance depends not only on the MB88F334 / MB88F336 package, but also on the characteristics of the PCB on which it is mounted.

The power consumption varies according to the application (i.e., this depends on the use case).

2.4. DC Limits

Latch-up may occur in a CMOS IC, if a voltage higher than (VDD, HVDD, VDP3 or VDP5) or less than (VSS) is applied to an input or output pin. Or, if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device.

Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

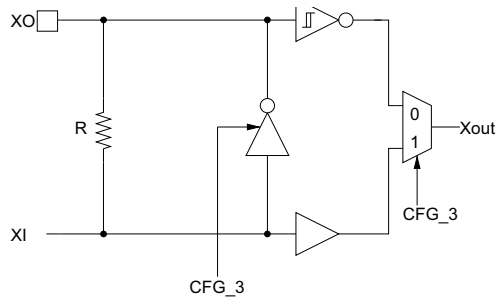
If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KOhm to 10KOhm) or enable internal pull-up or pull-down resistors.

The supply voltage to the I2C-BUS lines (SDA and SCL) must not exceed the power-supply voltage of this I/O cell (VDP5). You must not supply voltage to the I2C-BUS lines (SDA and SCL), if the power supply of this I/O cell (VDP5) is off.

2.5. IO Circuits

Table 2.6 shows the different IO circuit types used in MB88F334 and MB88F336. The different IO circuit types listed here correspond to the column D “Pin Type” in the attached file “Pinning.xlsx”.

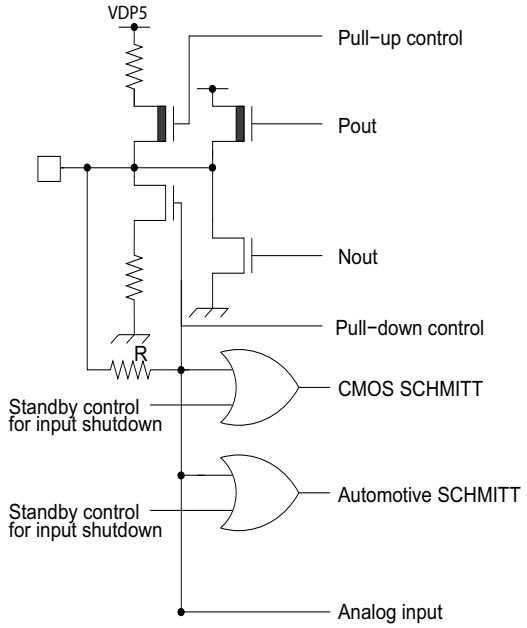
Table 2.6. : IO circuit types

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>OSC</td><td> 
</td><td>

VDEA-PLL IO supply domain
High-speed oscillation circuit
Programmable between oscillation mode (external crystal or resonator connected to XI/XO pins) and Clock input (CFG_3) mode (external clock connected to XI pin).
Input frequency: 30MHz APIX
Internal feedback resistor: 1MOhm (typ.)
Clock input mode (XI).
Please refer to the following table for this mode:

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8* VDEA_PLL</td><td></td><td>VDEA_PLL</td></tr>
<tr><td>VIL</td><td></td><td></td><td>0.2* VDEA_PLL</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-1µA</td><td></td><td>+1µA</td></tr>
</table>
</td></tr>
</table>

Table 2.6. : IO circuit types

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>BIDI50</td><td> 
</td><td>

VDP5 IO supply domain
CMOS output level

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>High output</td><td>VOH</td><td>VDP5-0.5V</td><td></td><td>VDP5</td></tr>
<tr><td>Low output</td><td>VOL</td><td>0V</td><td></td><td>0.4V</td></tr>
</table>

Programmable output drive strength

<table>
<tr><th>Drive Setting</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>00</td><td>IOL / IOH</td><td>± 1mA</td><td></td><td></td></tr>
<tr><td>01</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr>
<tr><td>10</td><td>IOL / IOH</td><td>± 5mA</td><td></td><td></td></tr>
<tr><td>11</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr>
</table>

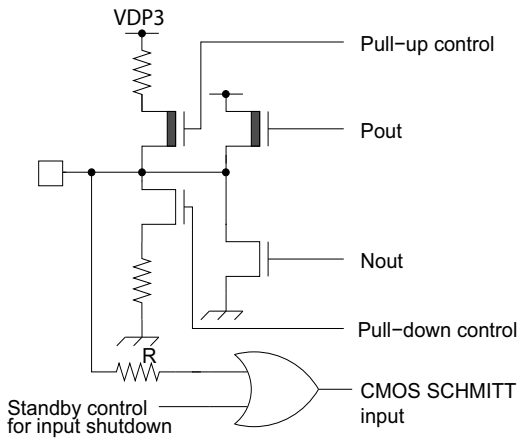
CMOS SCHMITT / Automotive SCHMITT input /Analog input

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP5</td><td></td><td>VDP5</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP5</td></tr>
<tr><td rowspan="2">Automotive</td><td>VIH</td><td>0.8*VDP5</td><td></td><td>VDP5</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.5*VDP5</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr>
</table>

Programmable pull-up and pull-down resistor

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Pull-up/ pull-down</td><td>R</td><td>25 kOhm</td><td>50 kOhm</td><td>100 kOhm</td></tr>
</table>
</td></tr>
</table>

Table 2.6. : IO circuit types

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr>
<td>BIDI33</td>
<td> 
</td>
<td>

VDP3 IO supply domain
CMOS level output

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>High output</td><td>VOH</td><td>VDP3-0.5V</td><td></td><td>VDP3</td></tr>
<tr><td>Low output</td><td>VOL</td><td>0V</td><td></td><td>0.4V</td></tr>
</table>

Output drive strength

<table>
<tr><th>Drive Setting</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td></td><td>IOL / IOH</td><td>± 4mA</td><td></td><td></td></tr>
</table>

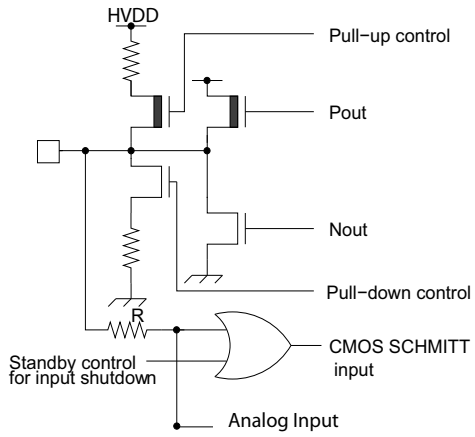
CMOS SCHMITT input

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP3</td><td></td><td>VDP3</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP3</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr>
</table>

Programmable pull-up and pull-down resistor

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Pull-up/ pull-down</td><td>R</td><td>15 kOhm</td><td>33 kOhm</td><td>70 kOhm</td></tr>
</table>
</td>
</tr>
</table>

Table 2.6. : IO circuit types

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>SMC</td><td> 
</td><td>

HVDD IO supply domain
CMOS output level

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>High output</td><td>VOH</td><td>HVDD-0.5V</td><td></td><td>HVDD</td></tr>
<tr><td>Low output</td><td>VOL</td><td>0V</td><td></td><td>0.4V</td></tr>
</table>

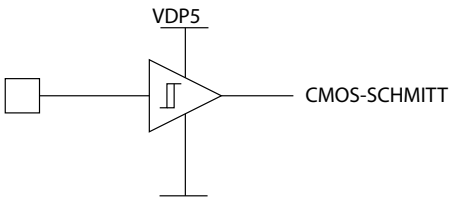
Programmable output drive strength

<table>
<tr><th>Drive Setting</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>00</td><td>IOL / IOH</td><td>± 1mA</td><td></td><td></td></tr>
<tr><td>01</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr>
<tr><td>10</td><td>IOL / IOH</td><td>± 30mA</td><td></td><td></td></tr>
<tr><td>11</td><td>IOL / IOH</td><td>± 5mA</td><td></td><td></td></tr>
</table>

CMOS SCHMITT / Analog input

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP5</td><td></td><td>VDP5</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP5</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr>
</table>

Programmable pull-up and pull-down resistor

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Pull-up/ pull-down</td><td>R</td><td>25 kOhm</td><td>50 kOhm</td><td>100 kOhm</td></tr>
</table>
</td></tr>
<tr><td>IN50</td><td> 
</td><td>

VDP5 IO supply domain
CMOS SCHMITT input

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP5</td><td></td><td>VDP5</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP5</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr>
</table>
</td></tr>
</table>

Table 2.6. : IO circuit types

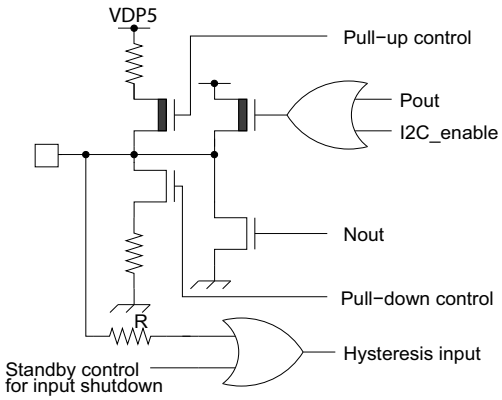
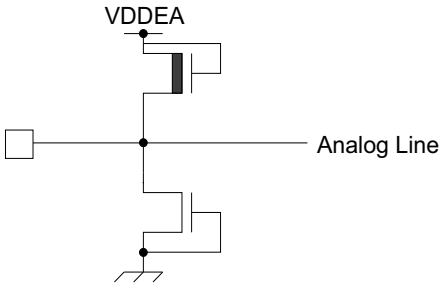
<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>I2C</td><td> 
</td><td>
■ VDP5 IO supply domain
■ CMOS output level
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>High output</td><td>VOH</td><td>VDP5-0.5V</td><td></td><td>VDP5</td></tr>
<tr><td>Low output</td><td>VOL</td><td>0V</td><td></td><td>0.4V</td></tr>
</table>
■ Programmable output drive strength
<table>
<tr><th>Drive Setting</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>00</td><td>IOL / IOH</td><td>± 1mA</td><td></td><td></td></tr>
<tr><td>01</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr>
<tr><td>10</td><td>IOL / IOH</td><td>± 5mA</td><td></td><td></td></tr>
<tr><td>11</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr>
<tr><td rowspan="2">*</td><td>IOL</td><td>± 3mA</td><td></td><td></td></tr>
<tr><td>IOH</td><td>(Pseudo Open drain) *1</td><td></td><td></td></tr>
<tr><td colspan="5">*1: For Pseudo Open Drain output logic value “1”, Push/Pull CMOS driver is switched to HIZ state.</td></tr>
</table>
■ CMOS SCHMITT (Automotive SCHMITT input / Analog input
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP5</td><td></td><td>VDP5</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP5</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr>
</table>
■ Programmable pull-up and pull-down resistor
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Pull-up/pull-down</td><td>R</td><td>25 kOhm</td><td>50 kOhm</td><td>100 kOhm</td></tr>
</table>
</td></tr>
<tr><td>AIO</td><td> 
</td><td>
■ VDDEA IO supply domain
■ Analog Pin
■ Type INPUT: Analog input pin with ESD protection
■ Type Output: Analog output line with ESD protection.
</td></tr>
</table>

Table 2.6. : IO circuit types

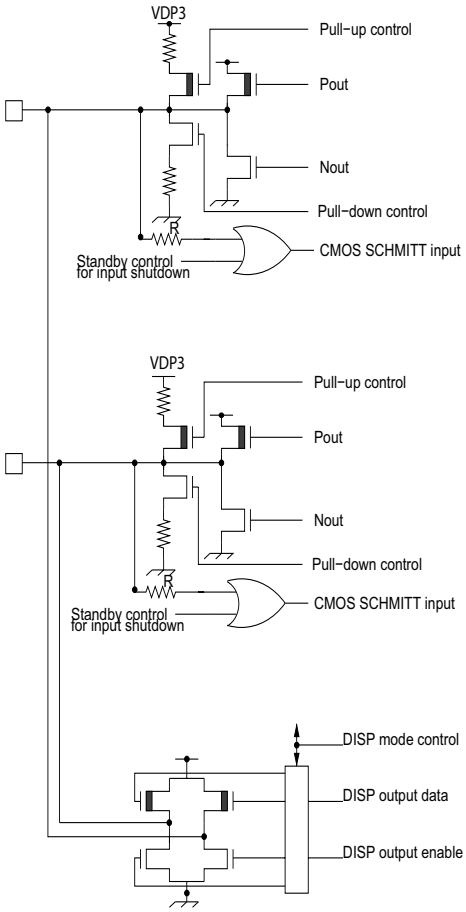
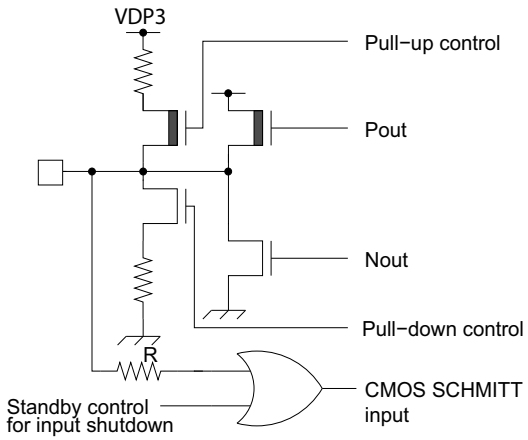
<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td rowspan="2">DISP_D</td><td> 
</td><td>■ VDP3 IO supply domain
■ CMOS output level
<table><tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>High output</td><td>VOH</td><td>VDP3-0.5V</td><td></td><td>VDP3</td></tr><tr><td>Low output</td><td>VOL</td><td>0V</td><td></td><td>0.5V</td></tr></table>■ Programmable output drive strength
<table><tr><th>Drive Setting</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>00</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr><tr><td>01</td><td>IOL / IOH</td><td>± 5mA</td><td></td><td></td></tr><tr><td>10</td><td>IOL / IOH</td><td>± 10mA</td><td></td><td></td></tr></table>■ CMOS SCHMITT input
<table><tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP3</td><td></td><td>VDP3</td></tr><tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP3</td></tr><tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr></table>■ Programmable pull-up/pull-down resistor
<table><tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Pull-up/pull-down</td><td>R</td><td>15kOhm</td><td>33kOhm</td><td>70kOhm</td></tr></table></td></tr>
<tr><td colspan="2">■ Differential output level
■ RSDS 100 Ohm Termination
<table><tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr><tr><td>Output differential voltage</td><td>VOD</td><td rowspan="3">Rload=100 Ohm
PAD_CTRLB: 0x0
(RSDS100)</td><td>150</td><td>250</td><td>350</td><td>mV</td></tr><tr><td>Output offset voltage</td><td>VOS</td><td>1.0</td><td>1.2</td><td>1.3</td><td>V</td></tr><tr><td>Output current amplitude</td><td>Iload100</td><td>1.5</td><td>2.5</td><td>3.5</td><td>mA</td></tr></table>■ RSDS 50 Ohm Termination
<table><tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr><tr><td>Output differential voltage</td><td>VOD</td><td rowspan="3">Rload=50 Ohm,
PAD_CTRLB: 0x2
(RSDS50 or LVDS)</td><td>125</td><td>175</td><td>225</td><td>mV</td></tr><tr><td>Output offset voltage</td><td>VOS</td><td>1.0</td><td>1.2</td><td>1.3</td><td>V</td></tr><tr><td>Output current amplitude</td><td>Iload50</td><td>2.5</td><td>3.5</td><td>4.5</td><td>mA</td></tr></table>■ LVDS
<table><tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr><tr><td>Output differential voltage</td><td>VOD</td><td rowspan="5">Rload=100 Ohm
PAD_CTRLB: 0x2
(RSDS50 or LVDS)</td><td>250</td><td>350</td><td>450</td><td>mV</td></tr><tr><td>Output offset voltage</td><td>VOS</td><td>1.125</td><td>1.25</td><td>1.375</td><td>V</td></tr><tr><td>Change to VOD</td><td>Vcod</td><td></td><td></td><td>50</td><td>mV</td></tr><tr><td>Change to VOS</td><td>Vcos</td><td></td><td></td><td>50</td><td>mV</td></tr><tr><td>Output current amplitude</td><td>Iload100</td><td>2.5</td><td>3.5</td><td>4.5</td><td>mA</td></tr></table></td></tr>
</table>

Table 2.6. : IO circuit types

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>DISP_S</td><td> 
</td><td>

VDP3 IO supply domain
CMOS output level

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>High output</td><td>VOH</td><td>VDP3-0.5V</td><td></td><td>VDP3</td></tr>
<tr><td>Low output</td><td>VOL</td><td>0V</td><td></td><td>0.5V</td></tr>
</table>

Programmable output drive strength

<table>
<tr><th>Drive Setting</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>00</td><td>IOL / IOH</td><td>± 2mA</td><td></td><td></td></tr>
<tr><td>01</td><td>IOL / IOH</td><td>± 5mA</td><td></td><td></td></tr>
<tr><td>10</td><td>IOL / IOH</td><td>± 10mA</td><td></td><td></td></tr>
<tr><td>11</td><td>IOL / IOH</td><td>± 30mA</td><td></td><td></td></tr>
</table>

CMOS SCHMITT input

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="2">CMOS</td><td>VIH</td><td>0.8*VDP3</td><td></td><td>VDP3</td></tr>
<tr><td>VIL</td><td>0V</td><td></td><td>0.2*VDP3</td></tr>
<tr><td>Input leakage</td><td>IL</td><td>-5µA</td><td></td><td>+5µA</td></tr>
</table>

Programmable pull-up/pull-down resistor

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>Pull-up/ pull-down</td><td>R</td><td>15 kOhm</td><td>33 kOhm</td><td>70 kOhm</td></tr>
</table>
</td></tr>
</table>

2.6. AC Limits

2.6.1. Host SPI Characteristics

2.6.1.1. Host SPI Interface

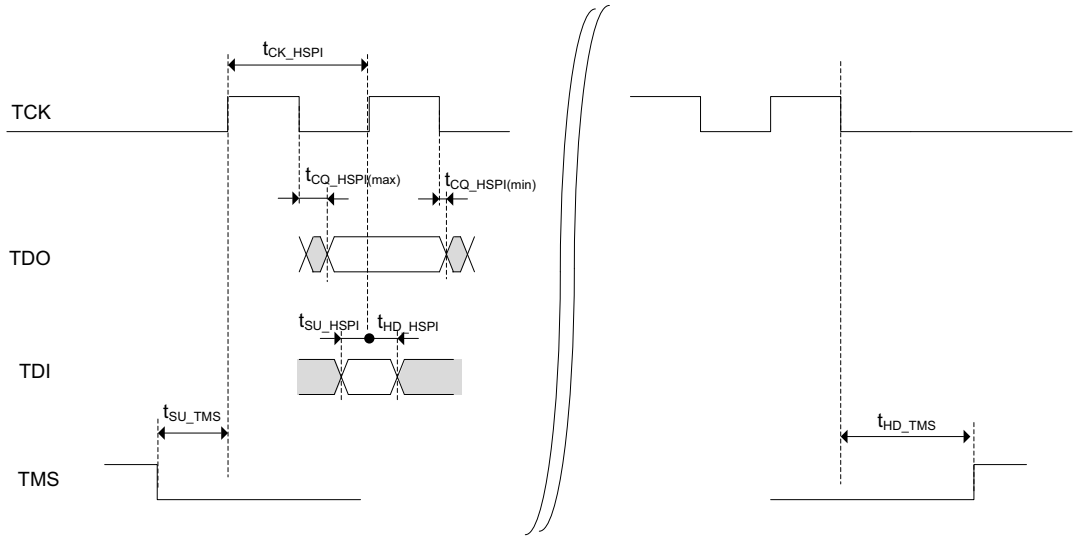


Figure 2.1. : Timing SPI Interface

Table 2.7. : AC Timing Host-SPI Interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
clk period	t_{CK_HSPI}	100			ns	Minimum 2x of HCLK period.
clk to output data	t_{CQ_HSPI}	0		20	ns	
Input data setup	t_{SU_HSPI}	10			ns	
Input data hold	t_{HD_HSPI}	5			ns	
Input Control setup	t_{HD_TMS}	50 + 2*tHCLK			ns	
Input Control Hold	t_{HD_TMS}	50 + 2*tHCLK			ns	

2.6.2. Config Interface

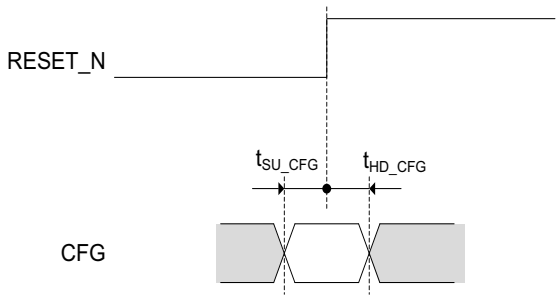


Figure 2.2. : Timing configuration pins

Table 2.8. : AC Timing configuration pjns

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
cfg data setup	t_{SU_CFG}	50			ns	
cfg data hold	t_{HD_CFG}	250			ns	

2.6.3. Display Interface

2.6.3.1. TTL Mode

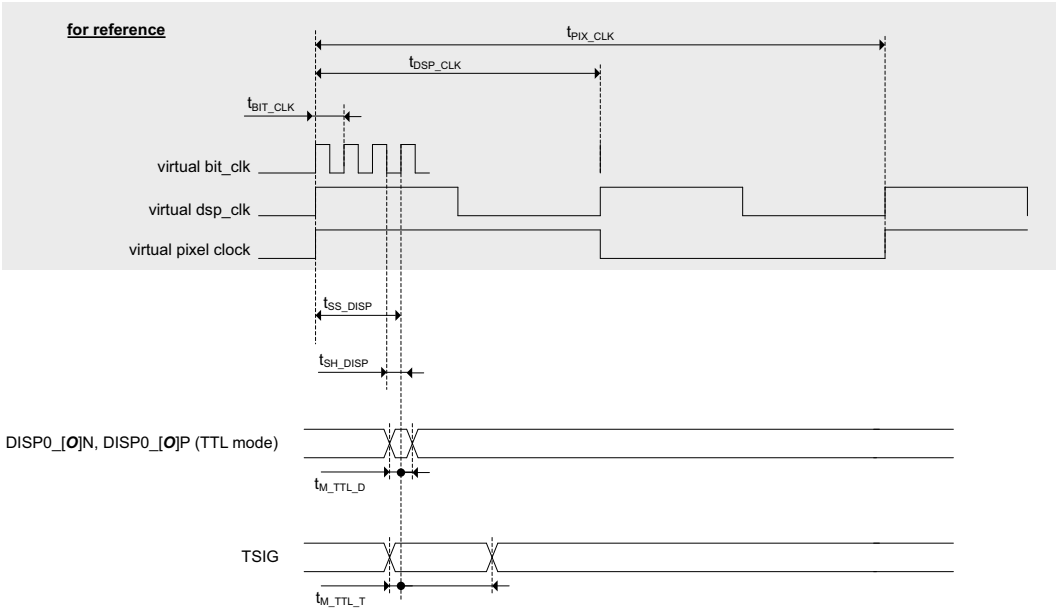


Figure 2.3. : Timing Display TTL Interface

Table 2.9. : AC Timing TTL Display Interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
dsp_clk period	t_{DSP_CLK}	5.5			ns	Internal clock for reference only
bit_clk period	t_{BIT_CLK}	1.8			ns	Internal clock for reference only, integer multiple of dsp_clk
Pixel clock period	t_{PIX_CLK}	11	11.7		ns	Typical value is maximum pixel frequency, minimum value is due to spread spectrum and clock synthesis
Shift value	t_{SS_DISP}	typ -150	$n \times t_{BIT\_CLK}$	typ +150	ps	
Half cycle shift	t_{SH_DISP}	typ -200	$\frac{t_{BIT\_CLK}}{2}$	typ +200	ps	
TTL DISP mismatch	$t_{M\_TTL\_D}$	-0.5		+0.5	ns	
TSIG TTL mismatch	$t_{M\_TTL\_T}$	1.5		4.5	ns	Related to center of DISP outputs

2.6.3.2. RSDS Mode

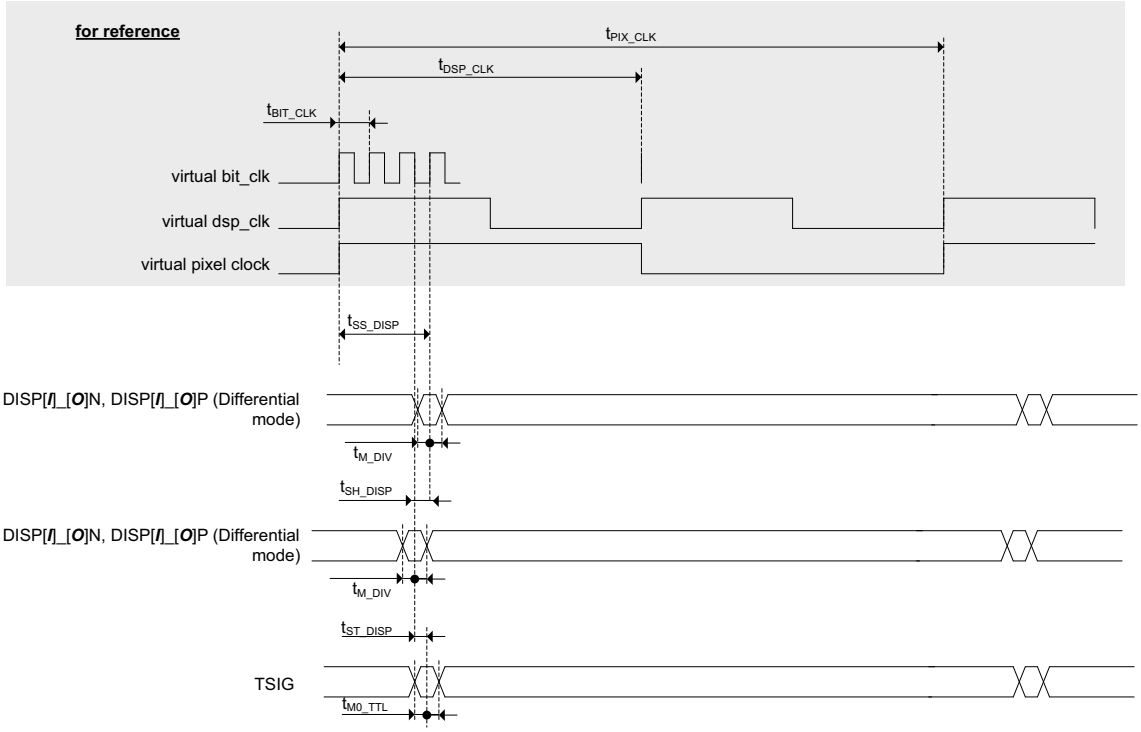


Figure 2.4. : Timing Display RSDS Interface

Table 2.10. : AC timings RSDS display interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
dsp_clk period	t_{DSP_CLK}	5.5			ns	Internal clock for reference only
bit_clk period	t_{BIT_CLK}	1.8			ns	Internal clock for reference only, integer multiple of dsp_clk
Pixel clock period	t_{PIX_CLK}	11	11.7		ns	Typical value is maximum pixel frequency, minimum value is due to spread spectrum and clock synthesis
Shift value	t_{SS_DISP}	typ-150	$n \times t_{BIT\_CLK}$	typ+150	ps	
Half cycle shift	t_{SH_DISP}	typ-200	$\frac{t_{BIT\_CLK}}{2}$	typ+200	ps	
TSIG output mismatch	t_{M_TTL}	-1.0		+1.0	ns	
RSDS to TSIG shift	t_{ST_DISP}	0.4	2.5	4.6	ns	
RSDS output mismatch	t_{M_DIV}	-0.5		+0.5	ns	

2.6.4. LVDS Interface

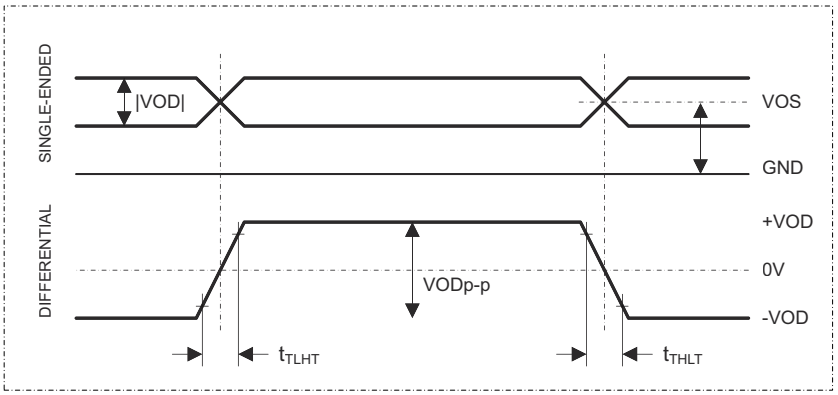


Figure 2.5. :

2.6.4.1. LVDS Interface Exceptions to TIA/EIA644 Specification

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Internal clock for reference only	bit_clk period	1905			ps	
Low to high transition time	t_{TLHT} *1) *2)		0.22	0.3	ns	RL=100 Ohm, CL=5pF
High to low transition time	t_{THLT} *1) *2)		0.22	0.3	ns	RL=100 Ohm, CL=5pF
Total Jitter at the data lanes	t_{TJ}*2		0.12	0.2	UI	

*1: Rise/fall times were determined using 20% and 80% of the voltage level respectively

*2: Specification is ensured by design and is not test in production

2.6.5. SPI Interface (External SPI and Flash SPI)

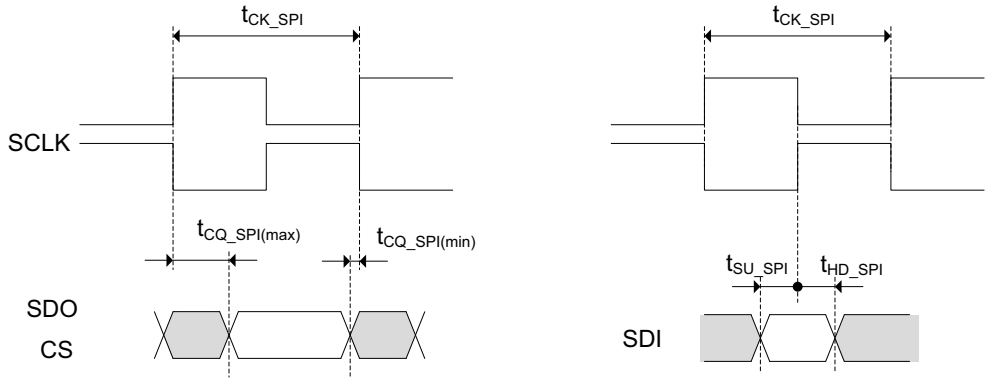


Figure 2.6. : Timing SPI Interface

Table 2.11. : AC Timings SPI Interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
clk period	t_{CK_SPI}	25			ns	Period depends on selected AHB clock or Peripheral clock frequency.
clk to output data	t_{CQ_SPI}	-4		9.5	ns	Active clock edge depends on interface setup.
input data setup	t_{SU_SPI}	 15 7.5			 ns ns	Active clock edge depends on interface setup. No re-timing mode. Re-timing mode.
input data hold	t_{HD_SPI}	 -3 2.5			 ns ns	Active clock edge depends on interface setup. No re-timing mode. Re-timing mode.

2.6.6. I2C Interface

The MB88F334 and MB88F336 fulfill the timing requirements for the standard mode and fast mode of the Philips I2C specification.

The supply voltage to the I2C-BUS lines (SDA and SCL) must not exceed the power-supply voltage of this I/O cell (VDP5).

You must not supply voltage to the I2C-BUS lines (SDA and SCL), if the power supply of this I/O cell (VDP5) is off.

2.6.7. USART/LIN Interface

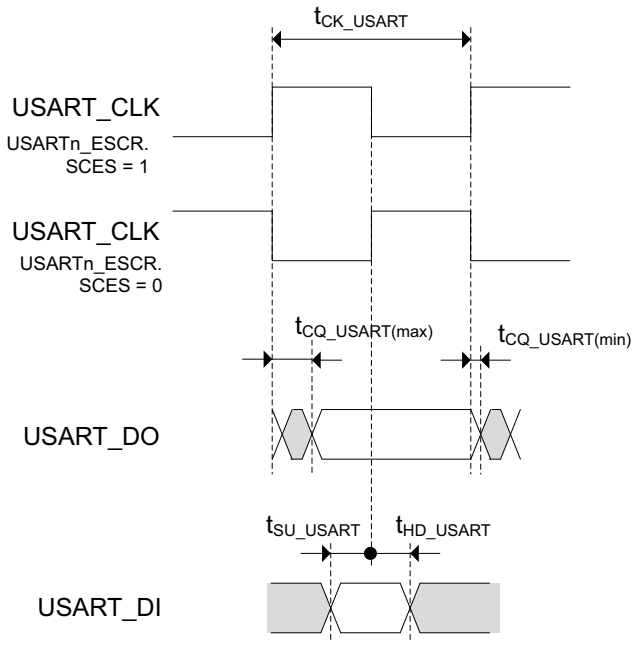


Figure 2.7. : Timing U(S)ART Interface

Table 2.12. : AC Timings U(S)ART Interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
CLK period	t_{CK_USART}	4 x t_{rbus_clk}			ns	
CLK to output data	t_{CQ_USART}	-5		20 2 x t_{rbus_clk} + 45	ns	Internal CLK mode External CLK mode
Input data setup	t_{SU_USART}	t_{rbus_clk} + 25			ns	
Input data hold	t_{HD_USART}	t_{rbus_clk}			ns	

2.6.8. I2S Interface

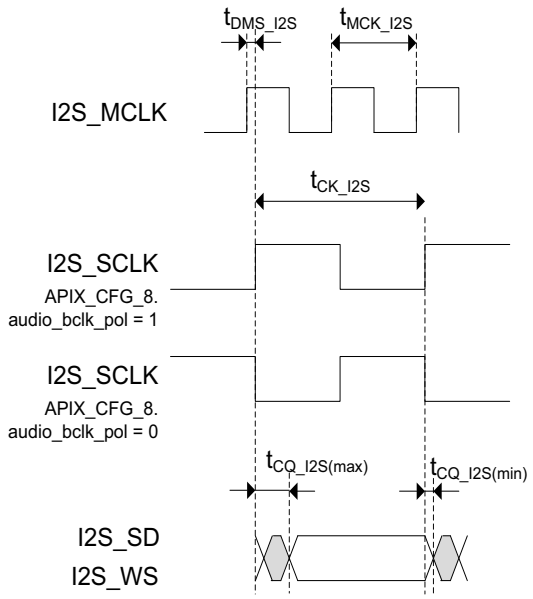


Figure 2.8. : Timing I2S Interface

Table 2.13. : AC timings I2S Interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
MCLK period	t_{MCK_I2S}	18.5			ns	
SCLK period	t_{CK_I2S}	37			ns	Half frequency of MCLK.
MCLK to SCLK delay	t_{DMS_I2S}	0		10	ns	
SCLK to output data	t_{CQ_I2S}	-5		10	ns	
(Requirement values. Have to be verified for customer data sheet)						

2.6.9. MII Interface

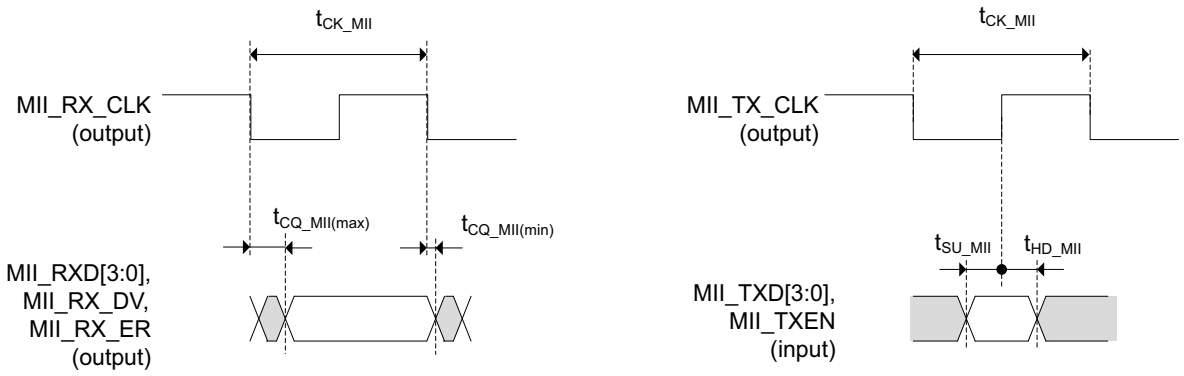


Figure 2.9. : Timing MII Interface in APIX IO mode (external Ethernet MAC connected)

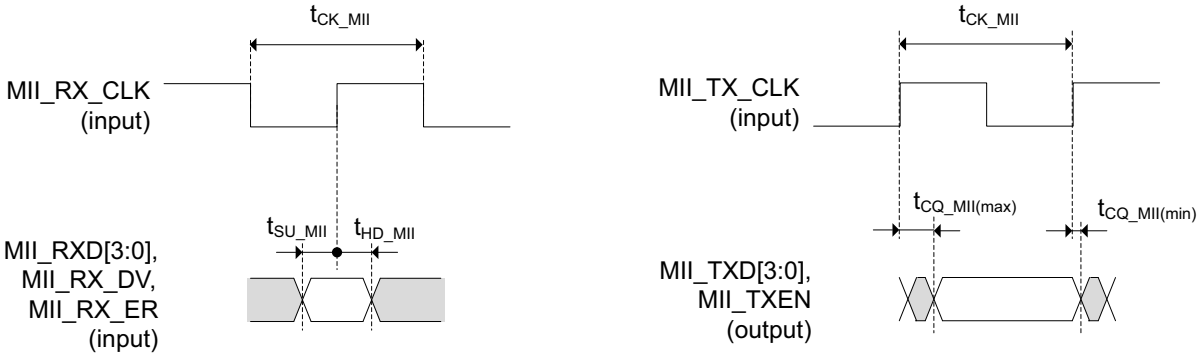


Figure 2.10. : Timing MII Interface in E2IP IO mode (external Ethernet PHY connected)

Table 2.14. : AC timings MII Interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
MII_CLK period	t_{CK_MII}		40 400		ns ns	100Mbit 10Mbit
Output delay	t_{CQ_MII}	0		10	ns	1)
Input data setup	t_{SU_MII}	20			ns	
Input data hold	t_{HD_MII}	0			ns	
1) For maximum drive strength setting						

2.7. Clock Input

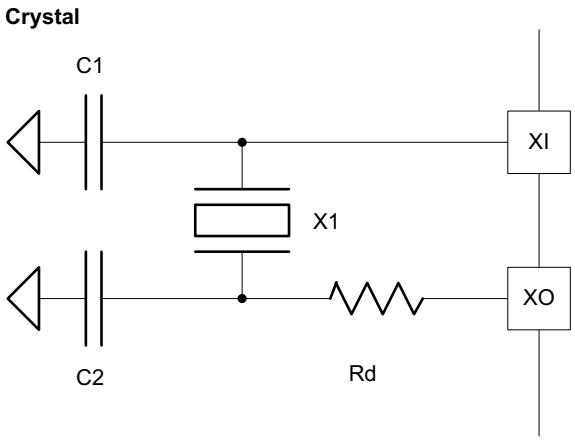


Figure 2.11. : Clock Input

Table 2.15. : Clock Input

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Crystal frequency	X1	-100 ppm	30	+100 ppm	MHz	
External load capacity	C1,C2		10		pF	Value depends on Crystal
Damping resistor	Rd		0		Ohm	If needed, value depends on Crystal
Coupling capacity	Cc		100		pF	
Input amplitude	V_{IH_XI}	0.8 * VDEA_PLL			V	If external clock is input at XI, see CFG_3 at section “2.5. Bootstrap Configuration”
	V_{IL_XI}			0.2 * VDEA_PLL	V	

2.8. Reset Timing

The low active reset input (RESET_N) has to be low for at least t_{RST}.

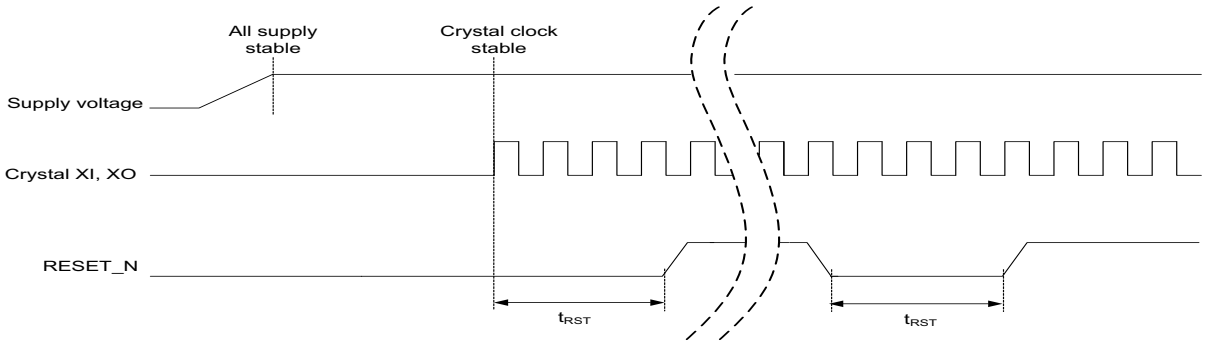


Figure 2.12. : Reset Timing

Table 2.16. : Clock Input

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset low time	t_{RST}	100			us	

2.9. Power-up

At any time, the difference between the power supply pins belonging to the same voltage level must not exceed 0.5V. This especially applies to the power on sequence. Otherwise, the risk of latchup will increase. Figure 2.13 shows the power on sequence and the groups of power supply that might be used, depending on the actual application. Furthermore, VDP5 supply must be switched on before any other power supply or at least at the same time.

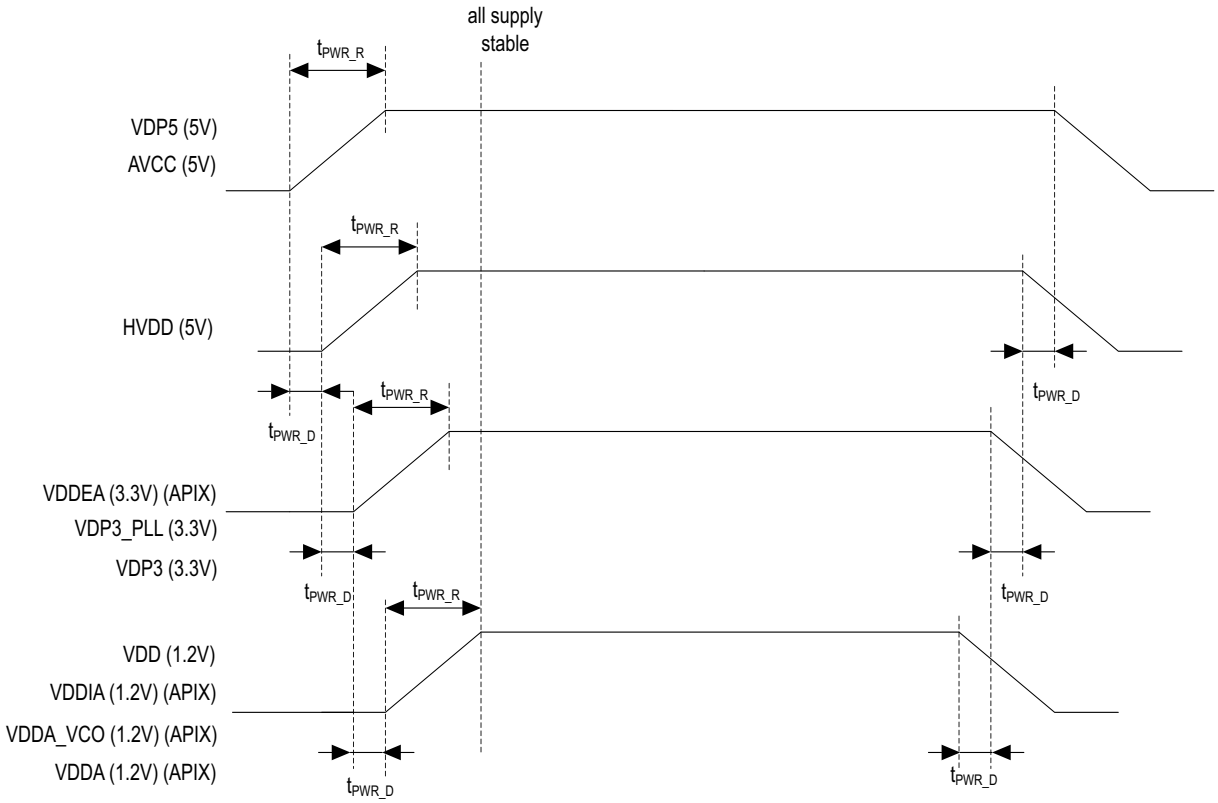


Figure 2.13. : Supply Power on Sequence

Table 2.17. : Timing power on

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Power Rise Time	t_{PWR_R}	0.05		30	ms	
Power Rise Delay	t_{PWR_D}	0		1	s	

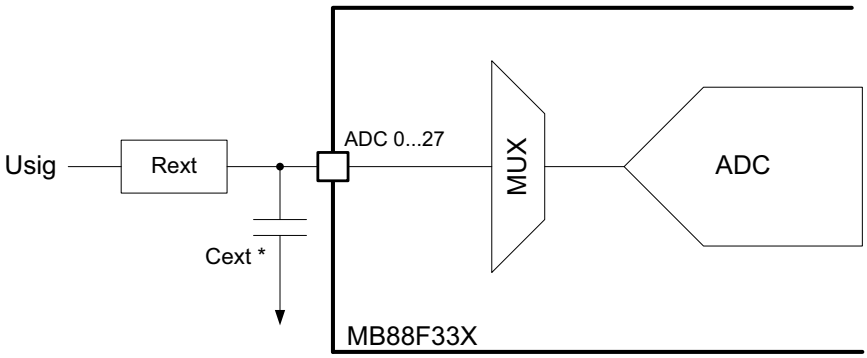
Note: The supply VDP5 has to be kept higher that VDD in all conditions.

2.10. ADC

2.10.1. Sampling Time

The MB88F334 and MB88F336 have (has) an embedded 10-bit successive approximation ADC with an internal integrated sampling and hold stage. The signal will charge the sampling capacitor at first and then the voltage signal on the sampling capacitor will be evaluated by the 10-bit ADC successively. The time to charge the sampling capacitor to its final value equal to the signal level is a function of the internal and external capacitor and resistor values. To reduce the error caused by the limited settling time to an acceptable level, the settling time should be chosen much larger than the time constant to charge the sampling capacitor. The settling time can be set with the ST register field of the CT register in the ADC register space.

The minimum sampling time can be calculated from the following formula:



* The ADC inputs should be bypassed with a capacitor 0.01-0.1 uF.
For details see application note: an-MB88F33X-SC1711-PCBDesignGuideline-rev2-30.

Figure 2.14. : ADC input signal

When VDP5 = HVDD = nominal 5V

For pins **ADC0 .. ADC15**:

$$Tsamp[min] = 7.63 \cdot [Rext \cdot (Cext + 16pF) + (Rext + 1.8k\Omega) \cdot 20pF]$$

Without external components:

$$Tsamp[min] = 275ns$$

For pins **ADC16 .. ADC27**:

$$Tsamp[min] = 7.63 \cdot [Rext \cdot (Cext + 16pF) + (Rext + 1.8k\Omega) \cdot 6pF + (Rext + 3.6k\Omega) \cdot 20pF]$$

Without external components:

$$Tsamp[min] = 632ns$$

When VDP5 = HVDD = nominal 3.3V

For pins **ADC0 .. ADC15**:

$$Tsamp[min] = 7.63 \cdot [Rext \cdot (Cext + 16pF) + (Rext + 4.3k\Omega) \cdot 20pF]$$

Without external components:

$$Tsamp[min] = 656ns$$

For pins **ADC16 .. ADC27**:

$$Tsamp[min] = 7.63 \cdot [Rext \cdot (Cext + 16pF) + (Rext + 4.3k\Omega) \cdot 6pF + (Rext + 8.6k\Omega) \cdot 20pF]$$

Without external components:

$$Tsamp[min] = 1.51\mu s$$

2.11. FLASH Memory Program/Erase Characteristics

Table 2.18. : Program/Erase Time

Parameter	Value			Unit	Remarks
	Min	Typ [1)]	Max		
Sector erase Time	-	0.3	1.5	s	The internal programming time before the erase procedure starts is included.
Macro Erase Time	-	1.2	12	s	
Word Programming Time	-	12	384	µs	

1) Typical definition: T_a=25°C / V_{DD}=1.2V / Program/Erase cycle= Immediately after shipment

Table 2.19. : Program/Erase Cycle and Data Retention Time [2)]

Program/Erase Cycle at Each Sector		Data Retention Time	
Min Value	Unit	Min Value	Unit
1000	cycles	20	years
10000	cycles	10	years
100000	cycles	5	years

2) These values were converted from the technology qualification using Arrhenius equation to translate high temperature measurements into normalized values at +85°C

Table 2.20. : Execution Time Limit

Parameter	Value [3)]	Unit
Program Execution Time Limit [4)]	1.3	ms
Macro Erase Execution Time Limit	62.4	s
Sector Erase Execution Time Limit [5)]	7.8	s

3) These values are development target values and may be changed depending on device evaluation results.

4) This is the time it takes for the macro to detect a ‘Hang-up 1’ error, when 1 is to be programmed to a memory cell, whose memory value is either 0 or X.5)

2.12. SMC Outputs

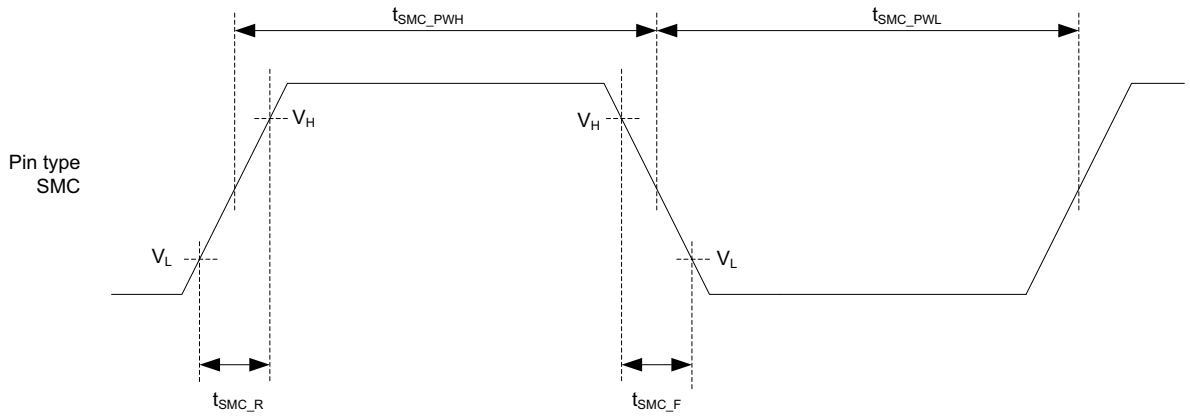


Figure 2.15. : Slew Rate of SMC output

Table 2.21. : SMC rise/fall time

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Rse/Fall Time	t_{SMC_R} t_{SMC_F}	15		100	ns	Min for C_{LOAD} = 0pF Max for C_{LOAD} = 100pF VH = 0.9 x HVDD VL = 0.1 x HVDD Output driving strength set to 30mA
Output Pulse Width	t_{SMC_PWH}	2.5			µs	Output driving strength set to 30mA
Output Pulse Width	t_{SMC_PWL}	2.5			µs	Output driving strength set to 30mA

2.13. Low Voltage Detection

The low voltage detection circuit supervises the core supply (VDD) and the GPIO supply (VDP5). Please refer to section “2.6.3. Low Voltage Detection (LVD)” in Chapter “Global Control”.

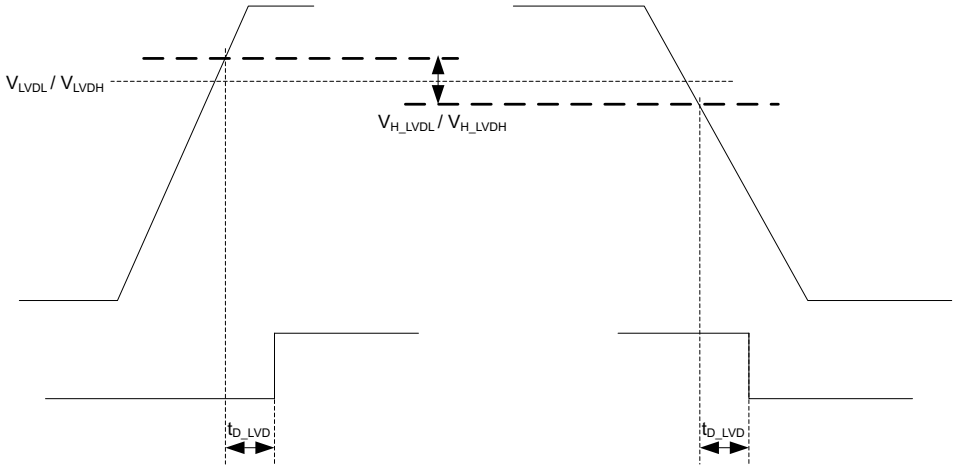


Figure 2.16. : Low voltage detection

Table 2.22. : Low voltage detection

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VDP5 detection voltage	V_{LVDH}	2.0	2.2	2.4	V	SVH setting = 0
		2.2	2.4	2.6	V	SVH setting = 1
		2.4	2.6	2.8	V	SVH setting = 3
		2.5	2.7	2.9	V	SVH setting = 2
		3.5	3.7	3.9	V	SVH setting = 6
		3.7	3.9	4.1	V	SVH setting = 7
		3.9	4.1	4.3	V	SVH setting = 5
		4.1	4.3	4.5	V	SVH setting = 4
VDP5 detection hysteresis	V_{H_LVDH}	75	100	150	mV	
VDD detection voltage	V_{LVDL}	0.4	0.5	0.6	V	SVL setting = 0
		0.5	0.6	0.7	V	SVL setting = 1
		0.6	0.7	0.8	V	SVL setting = 3
		0.7	0.8	0.9	V	SVL setting = 2
		0.8	0.9	1.0	V	SVL setting = 6
		0.9	1.0	1.1	V	SVL setting = 7
		1.0	1.1	1.2	V	SVL setting = 5
		1.1	1.2	1.3	V	SVL setting = 4
VDD detection hysteresis	V_{H_LVDL}	20	30	50	mV	
VDD/VDP5 detection delay	t_{D_LVD}			30	us	
Startup Time	t_{PU_LVD}			80	us	

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